Compal Confidential

VIWZ1/VIWZ2 DIS M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

nVIDIA N13P

2012-11-10

LA-9061P

REV:2.A

Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

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Size	Document Number	Rev
Custom	4019K3	C

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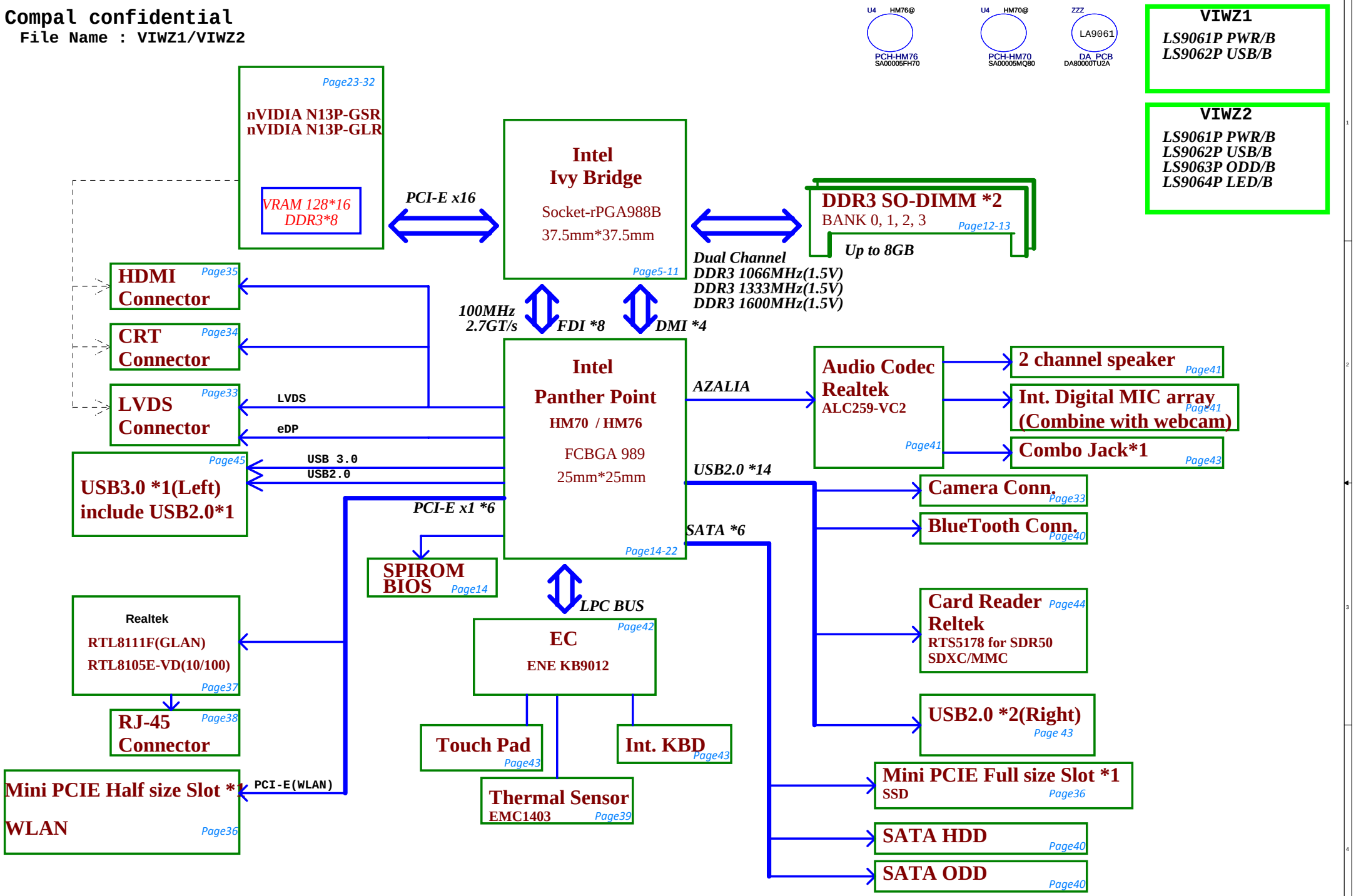
Compal confidential
File Name : VIWZ1/VIWZ2



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Voltage Rails

State \ power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	Porject	Phase
0	0	0 V	0 V	0 V	Z-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	Z-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	Z-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	Z-series	EVT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	Reserved	EVT
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	Reserved	DVT
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	Reserved	PVT
7	NC	2.500 V	3.300 V	3.300 V	Reserved	MP

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
USB Charger	1010 111X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

NV-GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111Xb (0x9E)

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB Port (Left Side) USB3.0
		1	Touch Screen
	UHCI1	2	Blue Tooth
		3	Camera
EHCI1	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Port (Right Side USB-BD)
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

BTO Item	BOM Structure
GPU:N13P-GS&GL	N13P@
OPTIMUS part	OPT@
integrate Graphic part	UMA@
GPU:N13P-GS&GSR	GS@
GPU:N13P-GL&GLR	GL@
GPU:N13P-GS Strap	GS1@
GPU:N13P-GL Strap	GL1@
GPU:N13P-GSR Strap	GSR@
GPU:N13P-GLR Strap	GLR@
OPTIMUS no support GCLK	OPTNOGCLK@
OPTIMUS support GCLK	OPTGCLK@
Support Green CLK	GCLK@
not Support Green CLK	NOGCLK@
Support Green CLK 244	GCLK244@
Support Green CLK 304	GCLK304@
Cardreader	CR@
Support HP Woofer	woofer@
Gastube	Gastube@
EC RESET function	RESET@
HDMI	HDMI@
BlueTooth	BT@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8105@
GIGA LAN	GIGA@
Deep Sleep S3	DS3@
Not Support Deep Sleep S3	NODS3@
ISCT	AOAC@
ISCT not support	NOAOAC@
Camera	CMOS@
For Z490 (14")	14@
For Z590 (15")	15@
Unpop	@
USB Charger	CHG@
not USBCharger	NOCHG@
Keyboard Back Light	KBL@
Touch Screen	TS@
HM76 by PCH	HM76@
HM70 by PCH	HM70@
Cardreader RTS5178	RTS5178@
Cardreader RTS5170	RTS5170@
for 14" Touch Screen	TS_14@
for 15" Touch Screen	TS_15@

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	TP
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS	X
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X	V +3VS
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X	X

GPU BOM Structure Table

BOM Structure	N13P-GS	N13P-GL	N13P-GSR	N13P-GLR
OPT@	V	V	V	V
OPTNOGCLK@	V	V	V	V
N13P@	V	V	V	V
GS@	V		V	
GL@		V		V
GS1@	V			
GL1@		V		
GSR@			V	
GLR@				V

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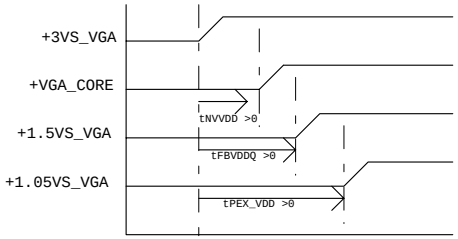
Hot plug detect for IFP link C

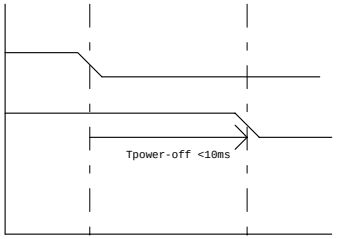
VGA and GDDR3 Voltage Rails (N13x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	N/A	
GPIO15	IN		Hot plug detect for IFP link C
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN		Hot Plug Detect for IFPE
GPIO19	IN	N/A	



1. all power rail ramp up time should be larger than 40us

2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ



1.all GPU power rails should be turned off within 10ms

Performance Mode P0 TDP at Tj = 102 C* (GDDR3)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13P-GL 64bit 1GB GDDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

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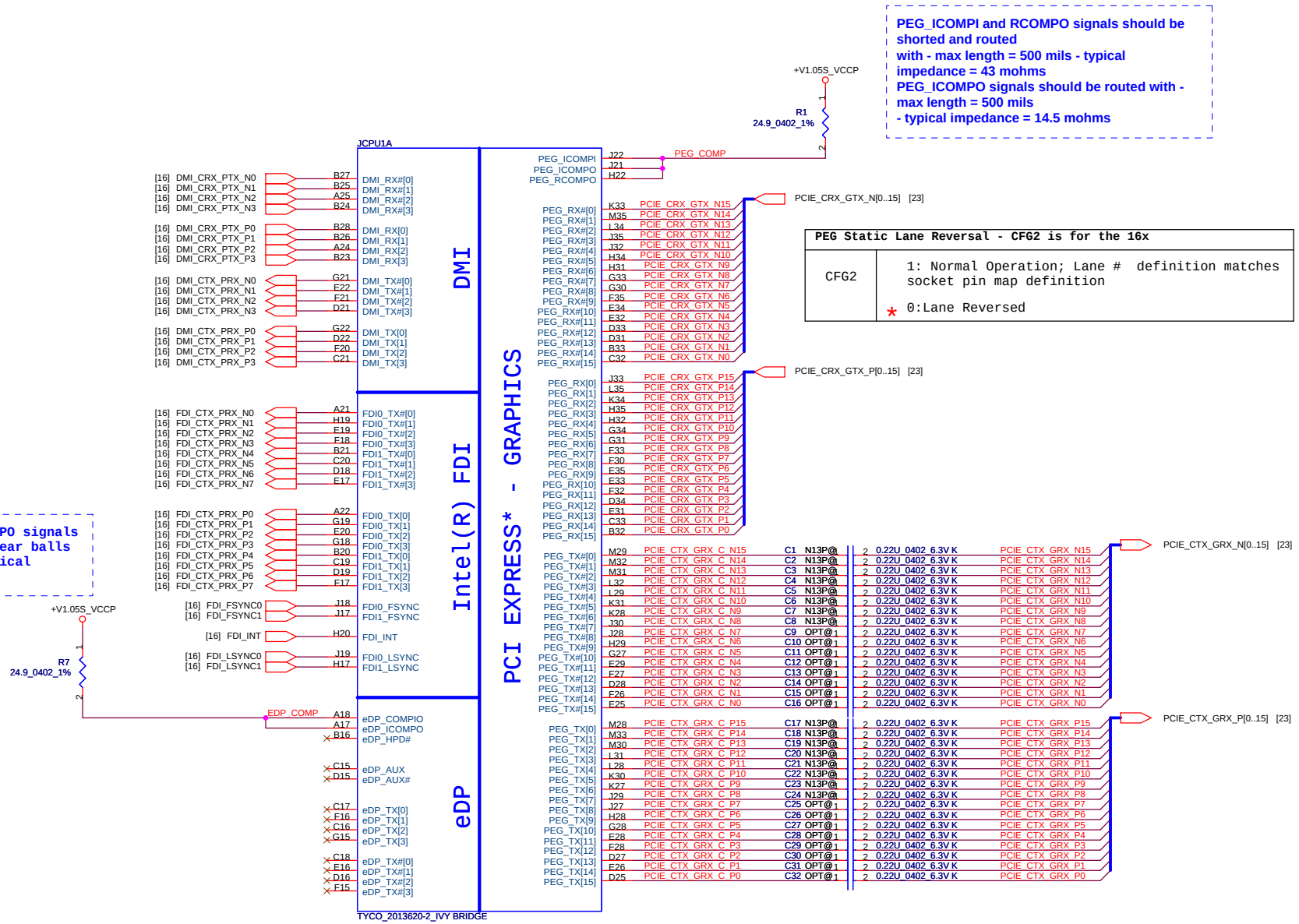

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

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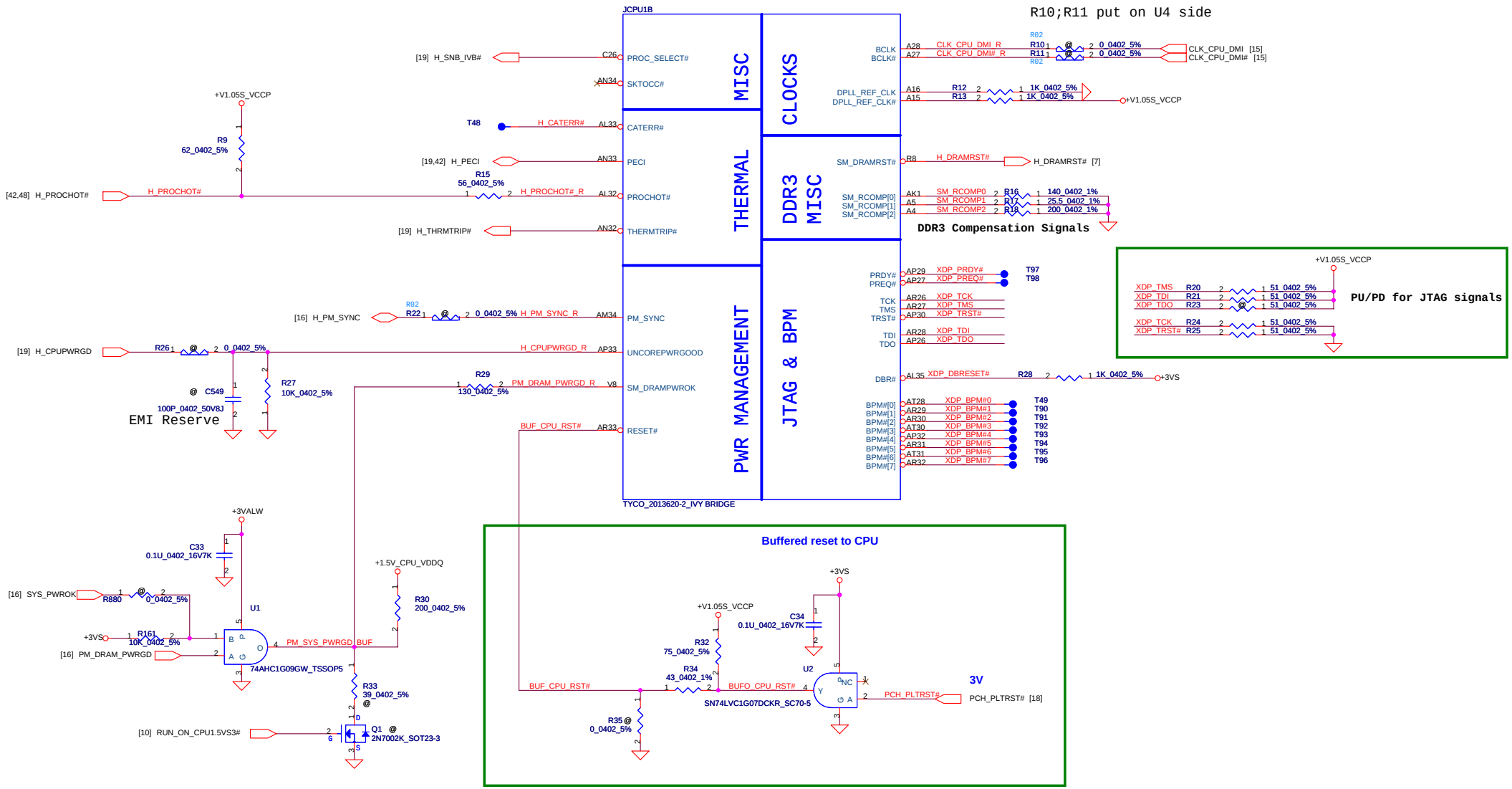

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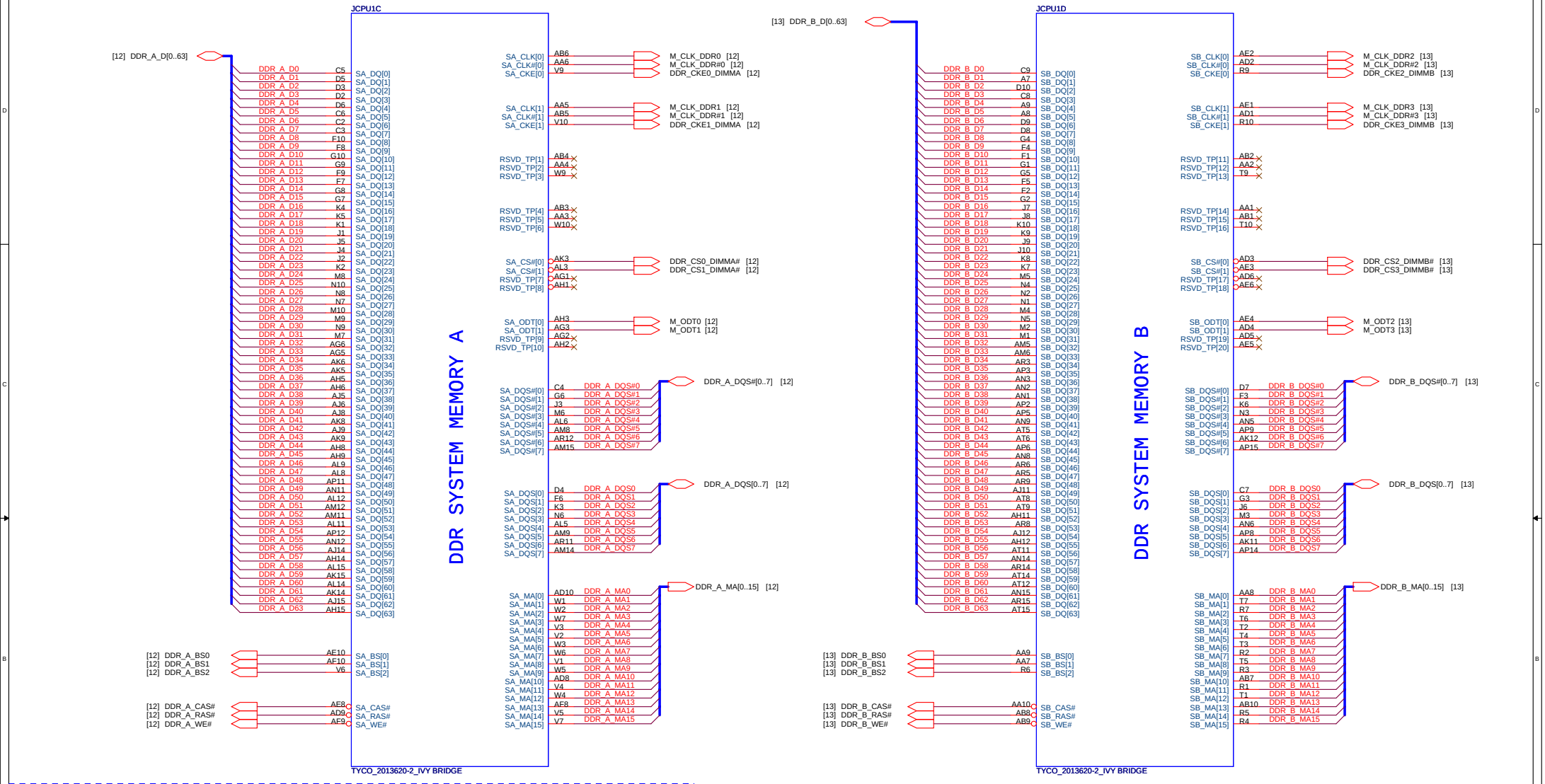

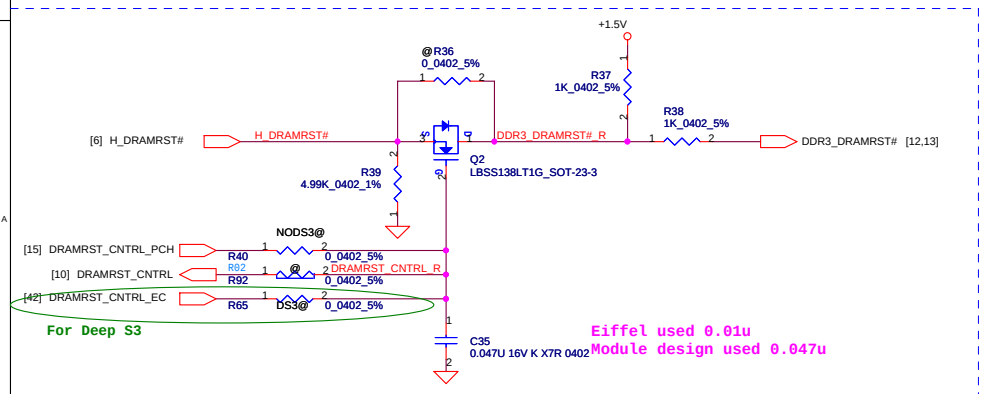

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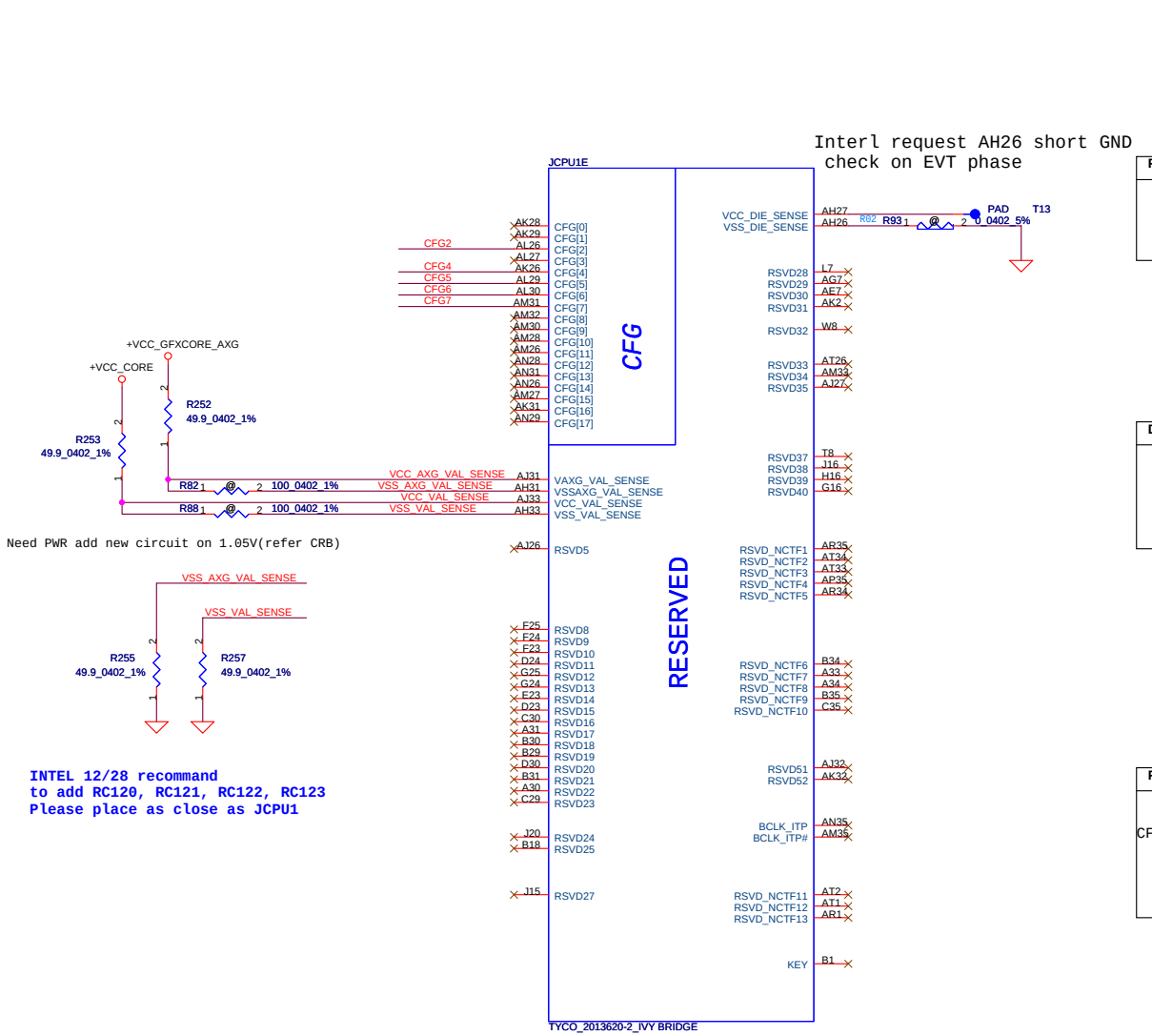
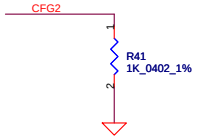
CFG Straps for Processor



Interl request AH26 short GND
check on EVT phase

INTEL 12/28 recommand
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1



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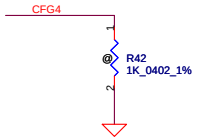
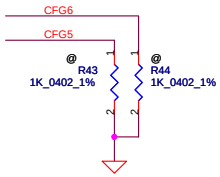
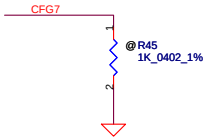
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

JCPU1F

+VCC_CORE

QC=94A
DC=53A

+V1.05S_VCCP

8.5A

CORE SUPPLY

AG35	VCC1
AG34	VCC2
AG33	VCC3
AG32	VCC4
AG31	VCC5
AG30	VCC6
AG29	VCC7
AG28	VCC8
AG27	VCC9
AG26	VCC10
AF35	VCC11
AF34	VCC12
AF33	VCC13
AF32	VCC14
AF31	VCC15
AF30	VCC16
AF29	VCC17
AF28	VCC18
AF27	VCC19
AF26	VCC20
AD35	VCC21
AD34	VCC22
AD33	VCC23
AD32	VCC24
AD31	VCC25
AD30	VCC26
AD29	VCC27
AD28	VCC28
AD27	VCC29
AD26	VCC30
AC35	VCC31
AC34	VCC32
AC33	VCC33
AC32	VCC34
AC31	VCC35
AC30	VCC36
AC29	VCC37
AC28	VCC38
AC27	VCC39
AC26	VCC40
AA35	VCC41
AA34	VCC42
AA33	VCC43
AA32	VCC44
AA31	VCC45
AA30	VCC46
AA29	VCC47
AA28	VCC48
AA27	VCC49
AA26	VCC50
Y35	VCC51
Y34	VCC52
Y33	VCC53
Y32	VCC54
Y31	VCC55
Y30	VCC56
Y29	VCC57
Y28	VCC58
Y27	VCC59
Y26	VCC60
V35	VCC61
V34	VCC62
V33	VCC63
V32	VCC64
V31	VCC65
V30	VCC66
V29	VCC67
V28	VCC68
V27	VCC69
V26	VCC70
U35	VCC71
U34	VCC72
U33	VCC73
U32	VCC74
U31	VCC75
U30	VCC76
U29	VCC77
U28	VCC78
U27	VCC79
U26	VCC80
R35	VCC81
R34	VCC82
R33	VCC83
R32	VCC84
R31	VCC85
R30	VCC86
R29	VCC87
R28	VCC88
R27	VCC89
R26	VCC90
P35	VCC91
P34	VCC92
P33	VCC93
P32	VCC94
P31	VCC95
P30	VCC96
P29	VCC97
P28	VCC98
P27	VCC99
P26	VCC100

PEG AND DDR

VCCIO1	AH13
VCCIO2	AH10
VCCIO3	AG10
VCCIO4	AC10
VCCIO5	Y10
VCCIO6	U10
VCCIO7	P10
VCCIO8	L10
VCCIO9	J14
VCCIO10	J13
VCCIO11	J12
VCCIO12	J11
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VCCIO24	E12
VCCIO25	E11
VCCIO26	D14
VCCIO27	D13
VCCIO28	D12
VCCIO29	D11
VCCIO30	C14
VCCIO31	C13
VCCIO32	C12
VCCIO33	C11
VCCIO34	B14
VCCIO35	B12
VCCIO36	A14
VCCIO37	A13
VCCIO38	A12
VCCIO39	A11
VCCIO40	J23

SVID

VIDALERT#	AJ29	H_CPU_SVIDALRT#	R47	43_0402_5%	VR_SVID_ALRT# [55]
VIDSCLK	AJ30	H_CPU_SVIDCLK	R02 R48	0_0402_5%	VR_SVID_CLK [55]
VIDSOUT	AJ28	H_CPU_SVIDDAT	R02 R49	0_0402_5%	VR_SVID_DAT [55]

+V1.05S_VCCP

C99
0.1U_0402_16V7K

R46
75_0402_5%

VR_SVID_CLK series-resistors close to VR

R50 130_0402_5% +V1.05S_VCCP 0.1uF on power side

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

SENSE LINES

Trace Impedance =27-33 ohm
Trace Length Matc < 25 mils

+VCC_CORE

R51
100_0402_1%

VCC_SENSE	AJ35	VCCSENSE_R	R02 R52	0_0402_5%
VSS_SENSE	AJ34	VSSSENSE_R	R02 R53	0_0402_5%

VCCSENSE [55]
VSSSENSE [55]

VCCIO_SENSE	B10			
VSS_SENSE_VCCIO	A10	VSSIO_SENSE_L	R74 10_0402_1%	VSSIO_SENSE

VCCIO_SENSE [53]

R66 100_0402_1%

R54
100_0402_1%

R74 & R79 put together

+V1.05S_VCCP

R79
10_0402_1%

VSSIO_SENSE_L [53]

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

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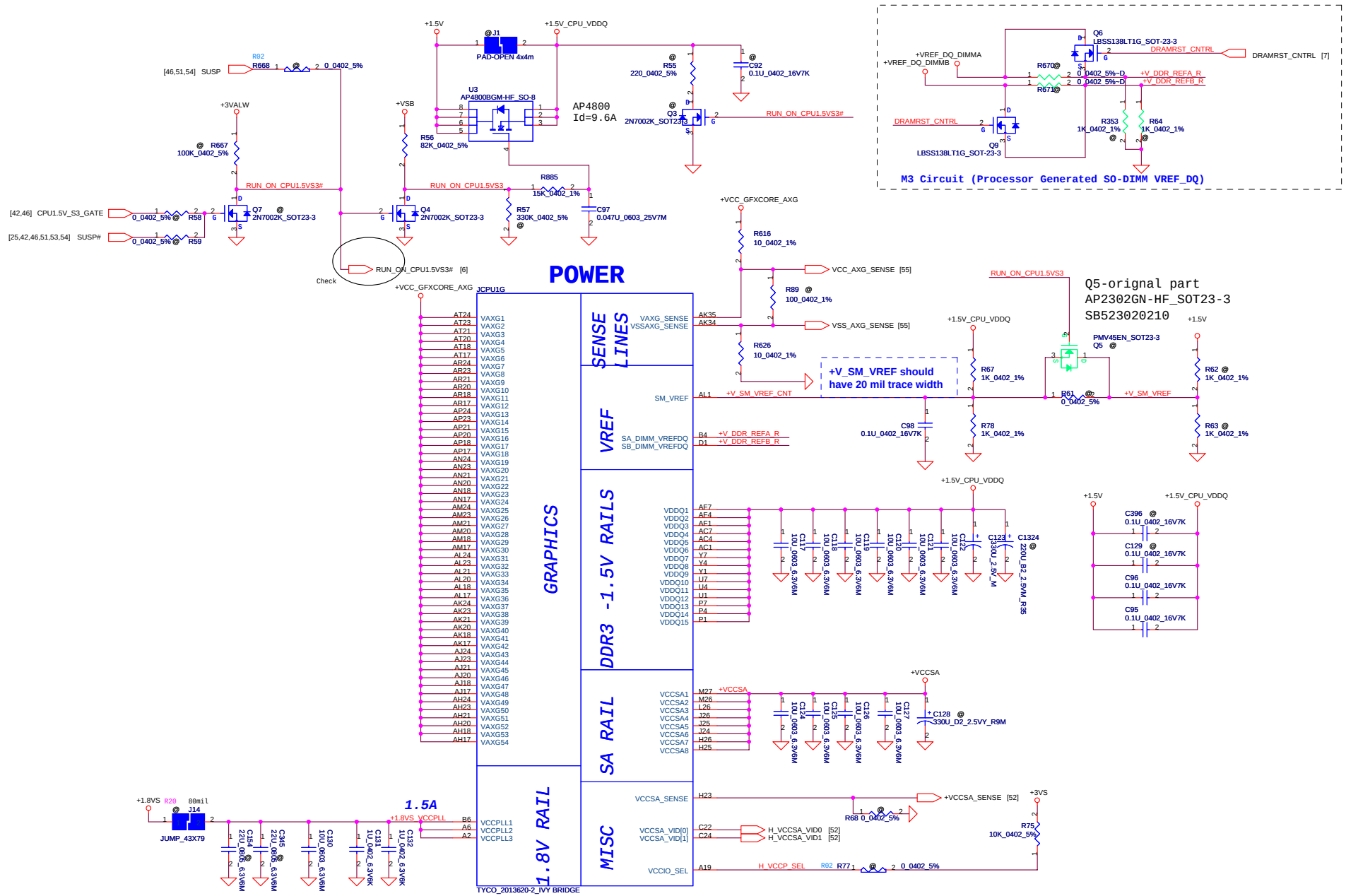

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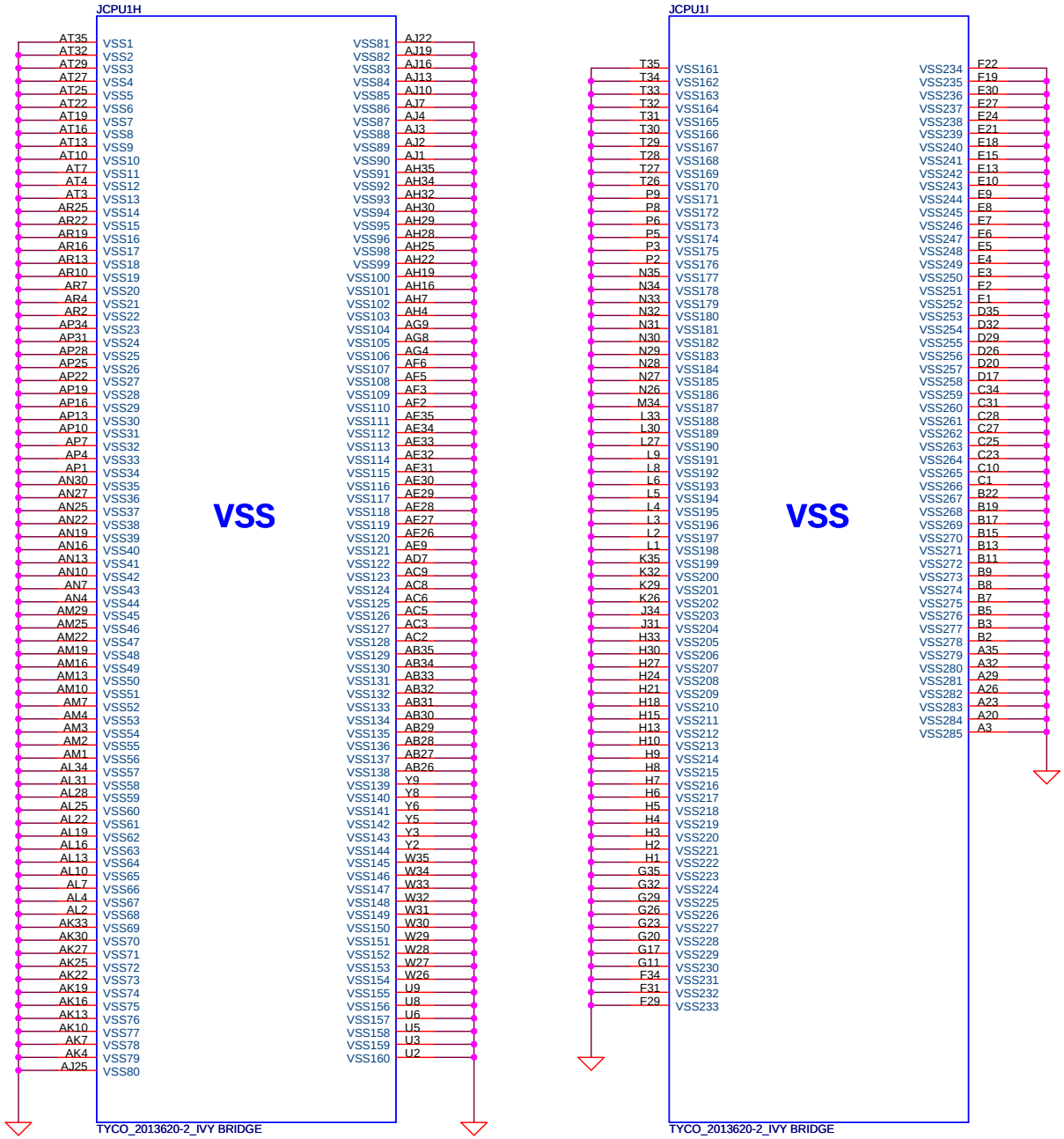

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DDR3 SO-DIMM A

JDIMM1

LCN_DAN06-K4806-0103

ME@

[7] DDR_A_D[0..63]
[7] DDR_A_DQS[0..7]
[7] DDR_A_DQS#[0..7]
[7] DDR_A_MA[0..15]

DDR3_DRAMRST# [13,7]
[7] DDR_CKE0_DIMMA
[7] DDR_A_BS2
[7] M_CLK_DDR0
[7] M_CLK_DDR#0
[7] DDR_A_BS0
[7] DDR_A_WE#
[7] DDR_A_CAS#
[7] DDR_CS1_DIMMA#
DDR_CKE1_DIMMA [7]
M_CLK_DDR1 [7]
M_CLK_DDR#1 [7]
DDR_A_BS1 [7]
DDR_A_RAS# [7]
DDR_CS0_DIMMA# [7]
M_ODT0 [7]
M_ODT1 [7]
SMB_DATA_S3 [13,15,36,43]
SMB_CLK_S3 [13,15,36,43]

R70 1K_0402_1%
R71 1K_0402_1%
R72 1K_0402_1%
R73 1K_0402_1%
R81 10K_0402_5%
R83 10K_0402_5%

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

EVT Check

Layout Note:
Place near DIMM

7/28 Update connect GND directly

Layout Note:
Place near DIMM

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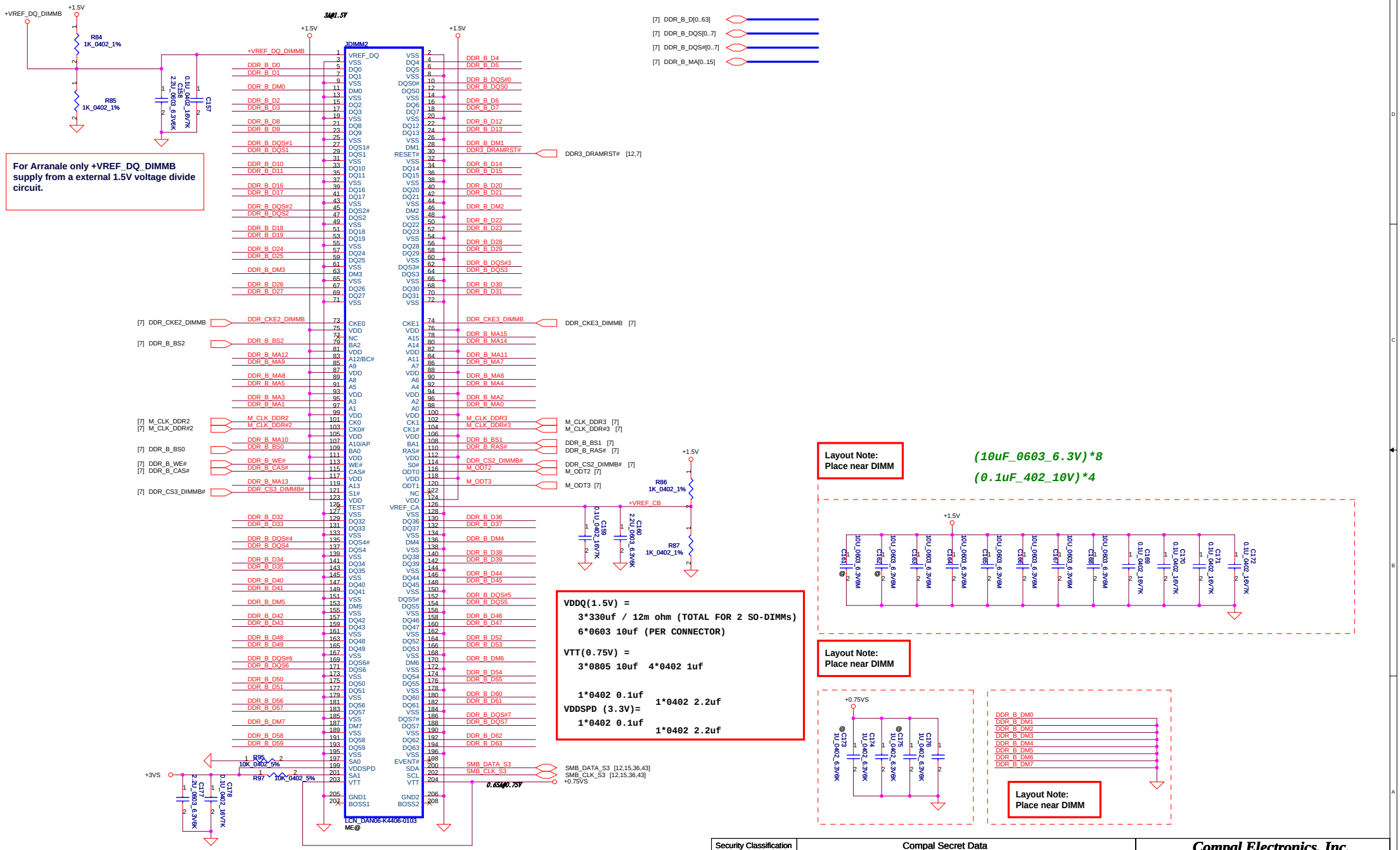

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6*0603 10uf (PER CONNECTOR)

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3*0805 10uf 4*0402 1uf

1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

Layout Note: Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note: Place near DIMM

Layout Note: Place near DIMM

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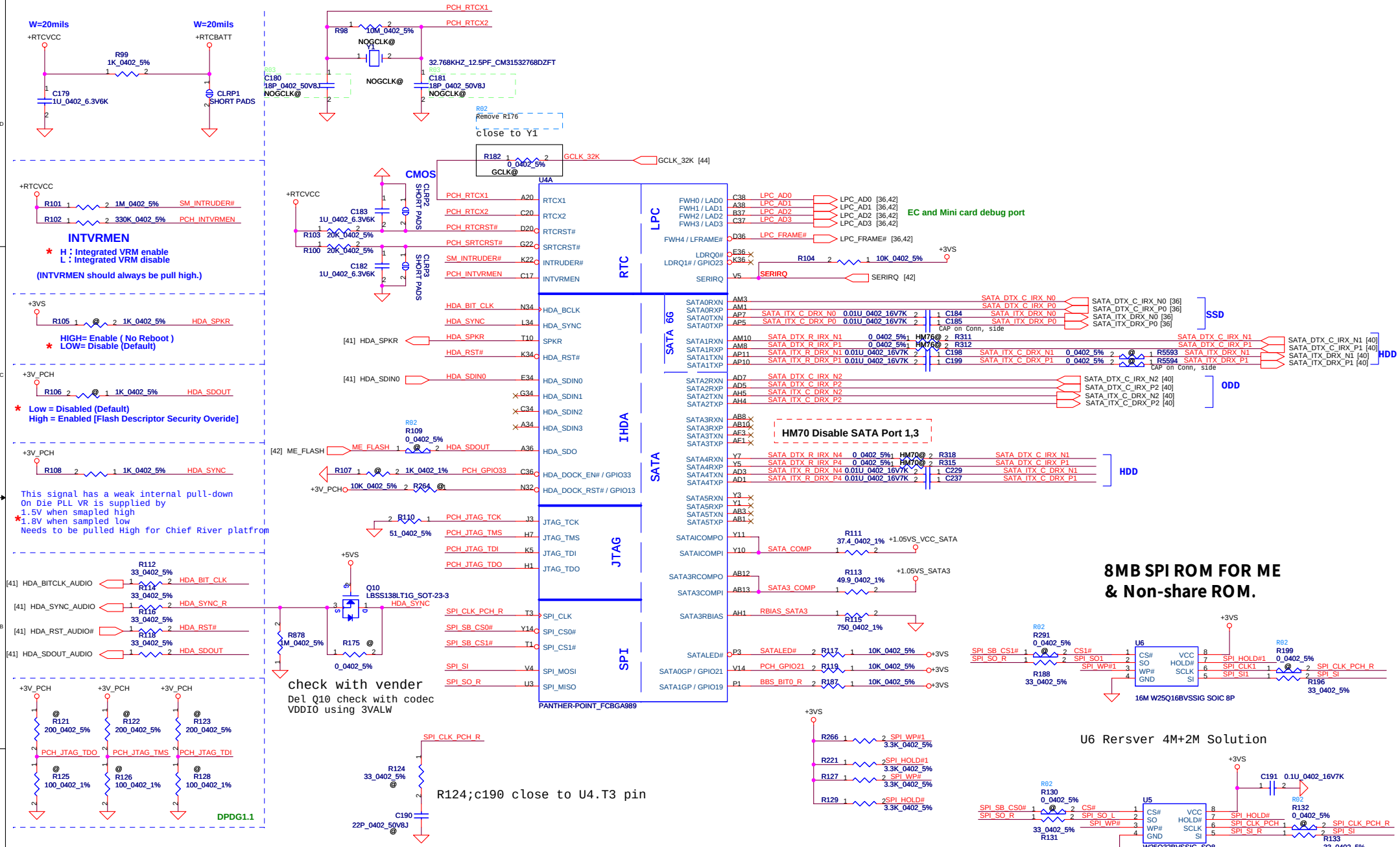

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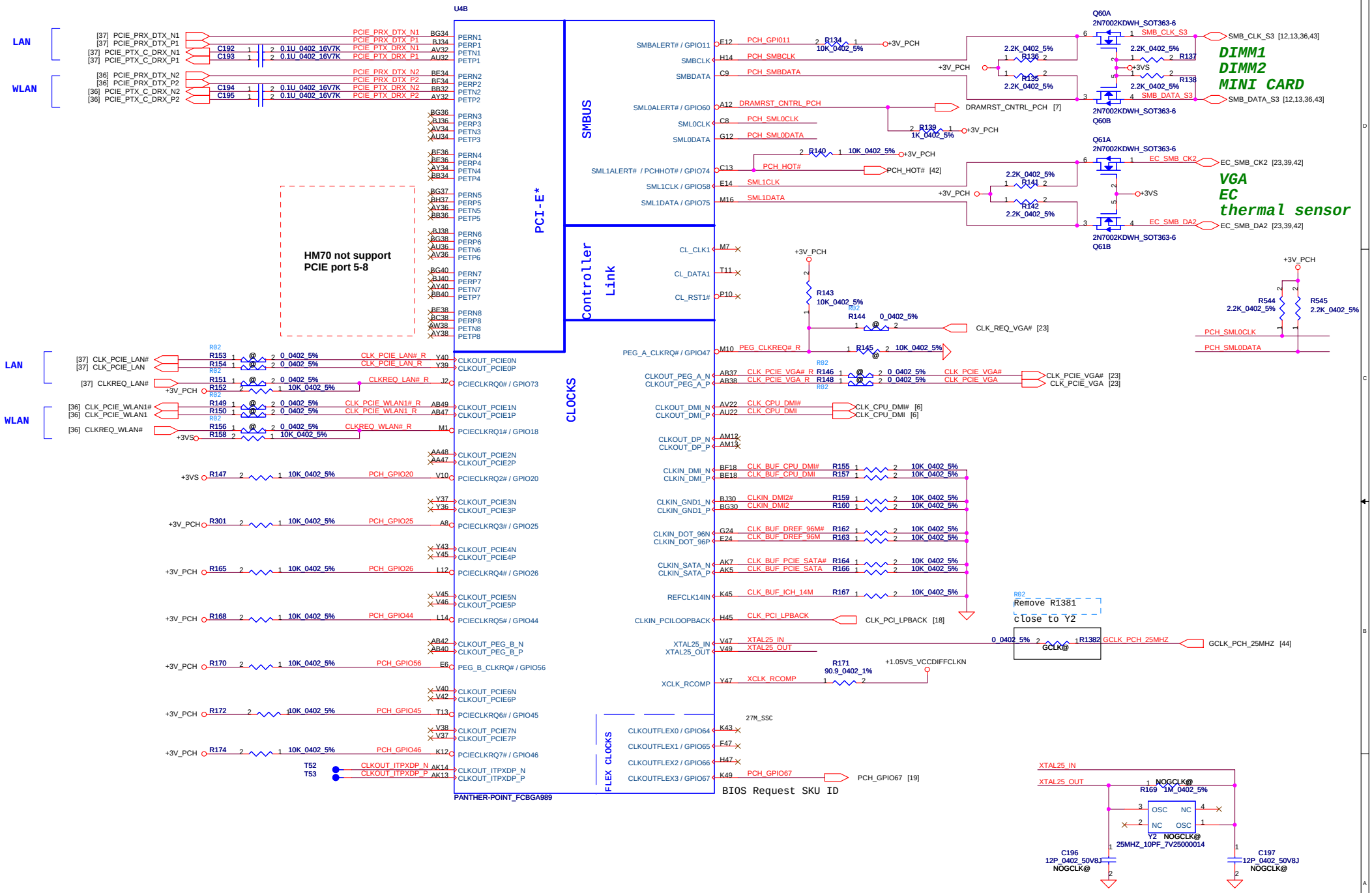

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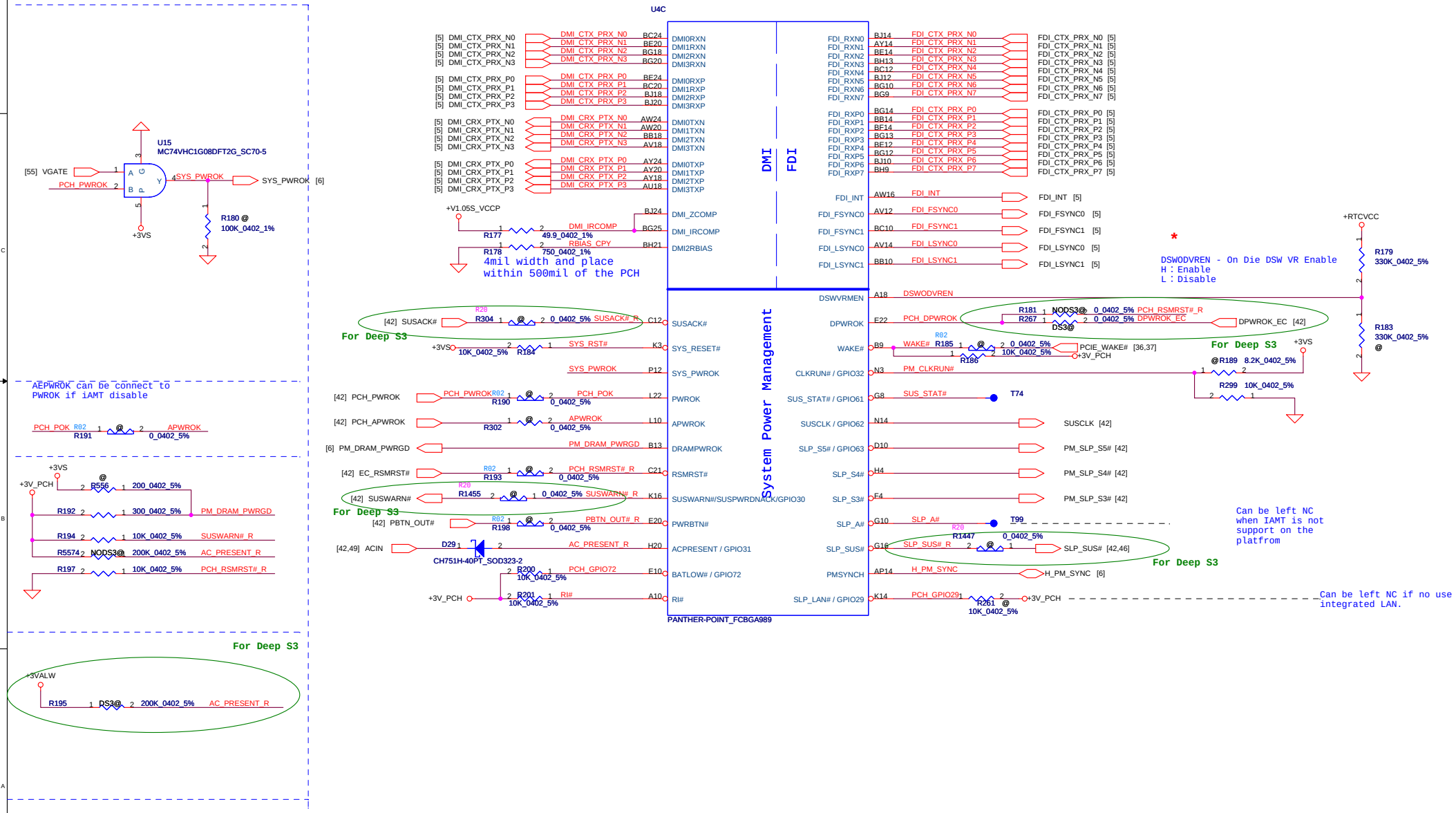

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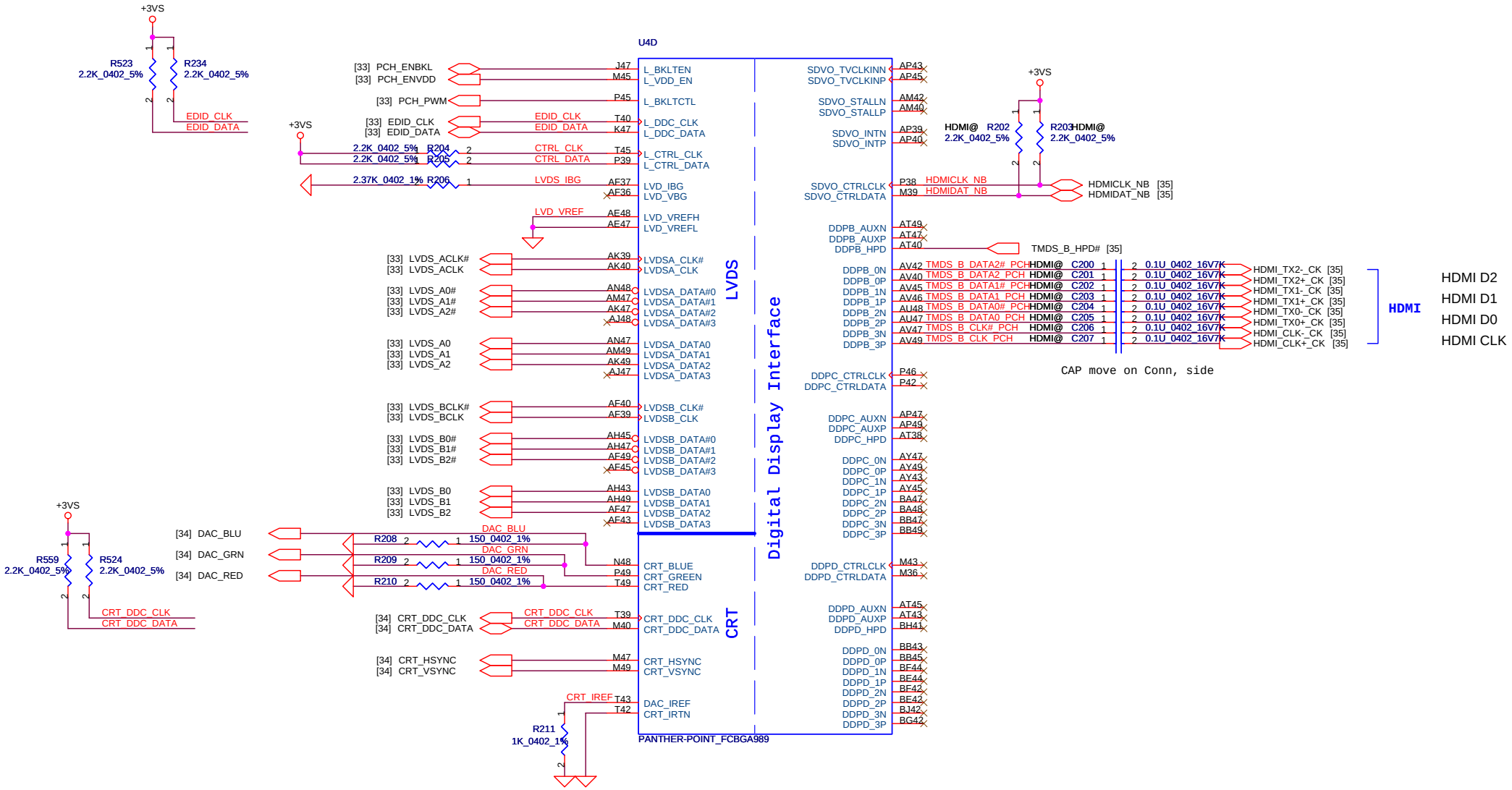

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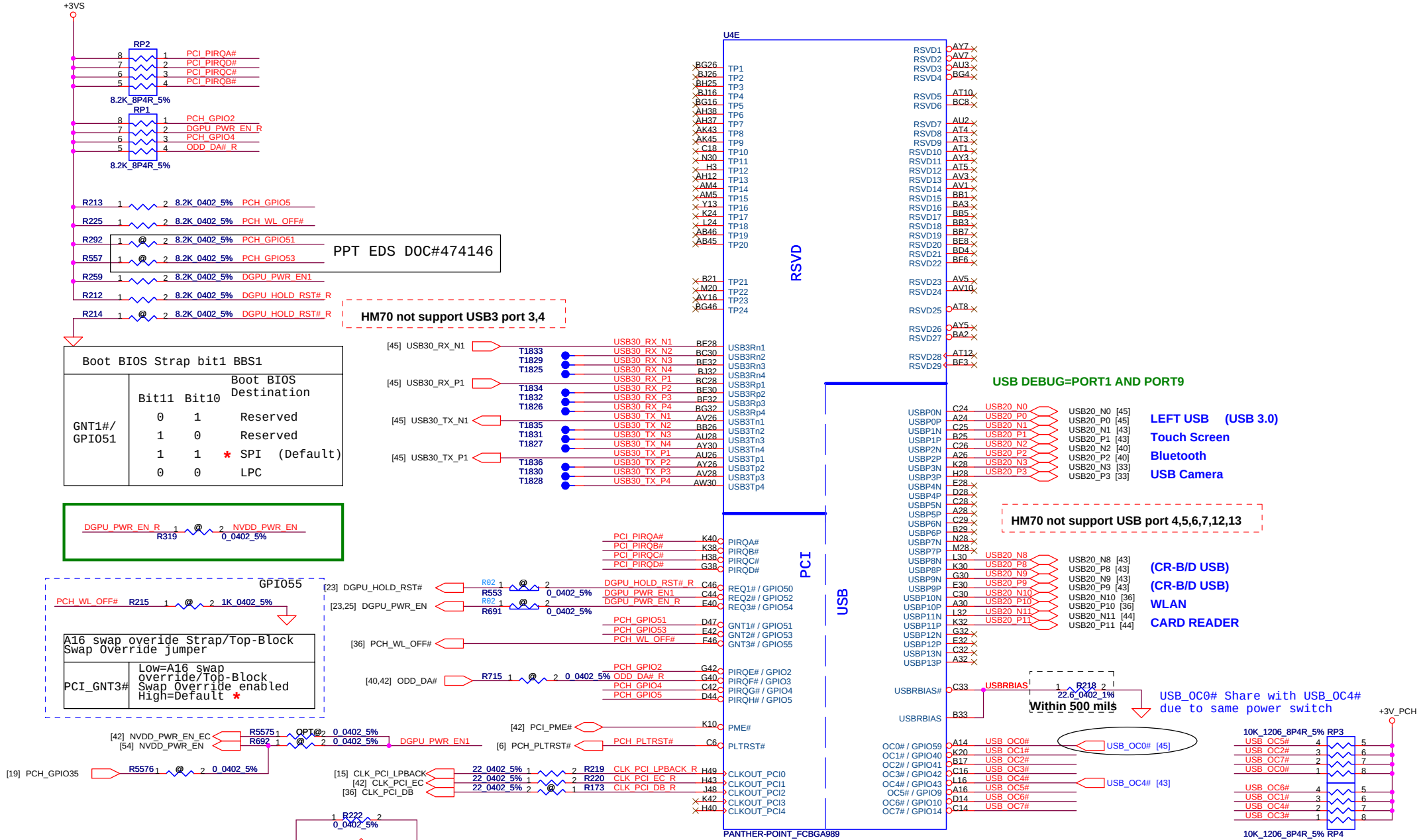

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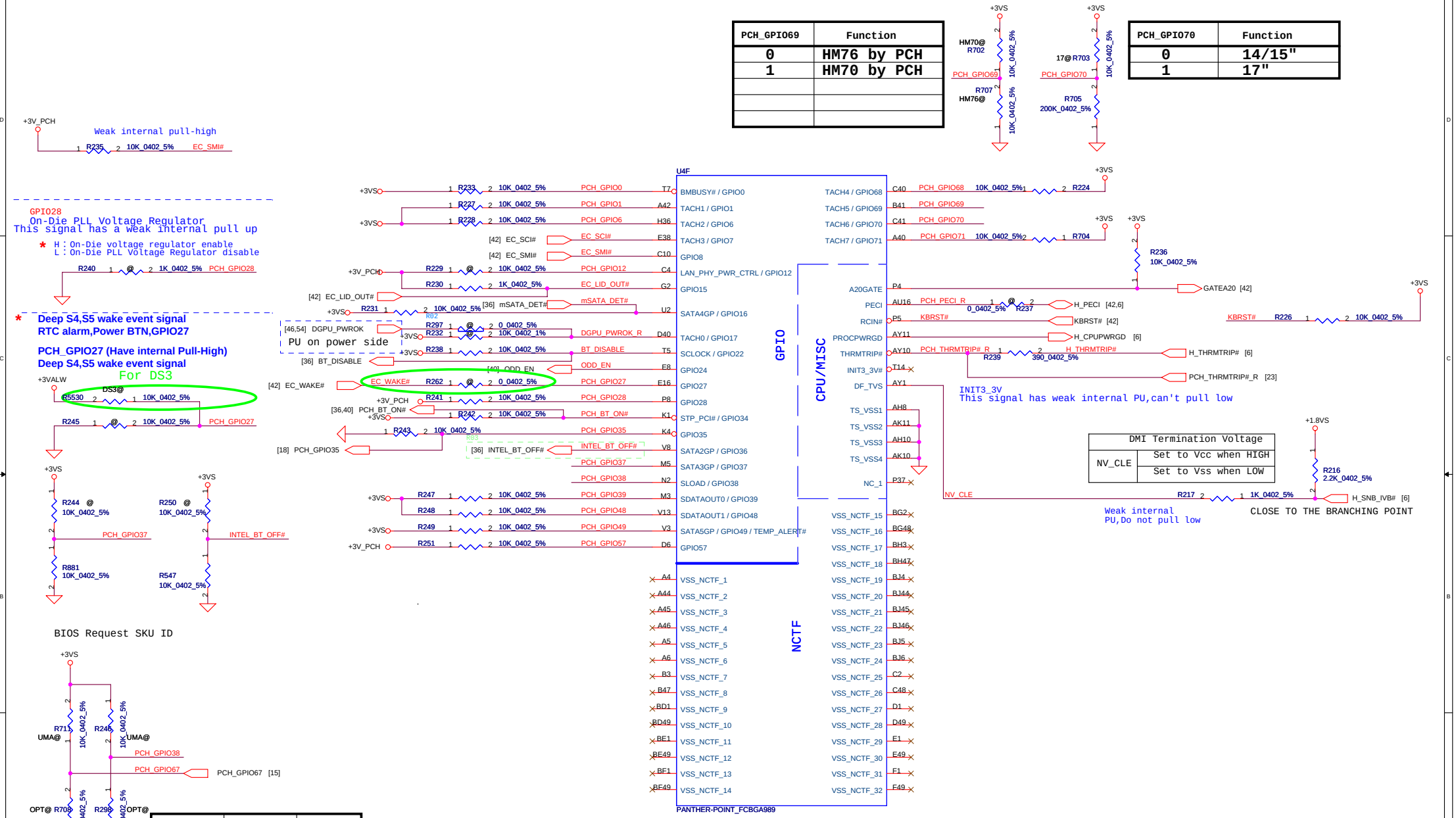
PCH_GPIO69	Function
0	HM76 by PCH
1	HM70 by PCH

PCH_GPIO70	Function
0	14/15"
1	17"



PCH_GPIO38	PCH_GPIO67	Function
0	0	Optimus
1	1	UMA

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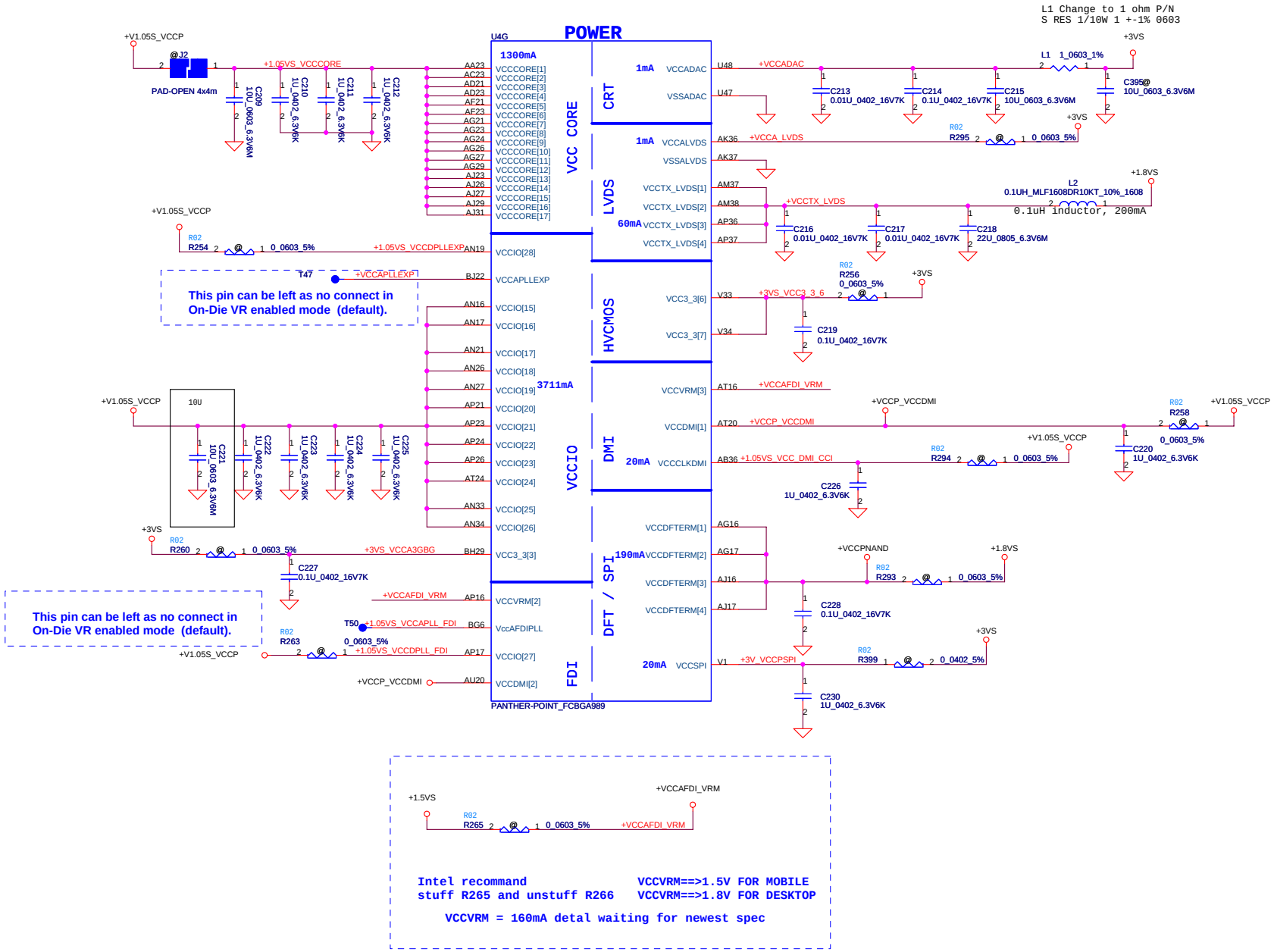

PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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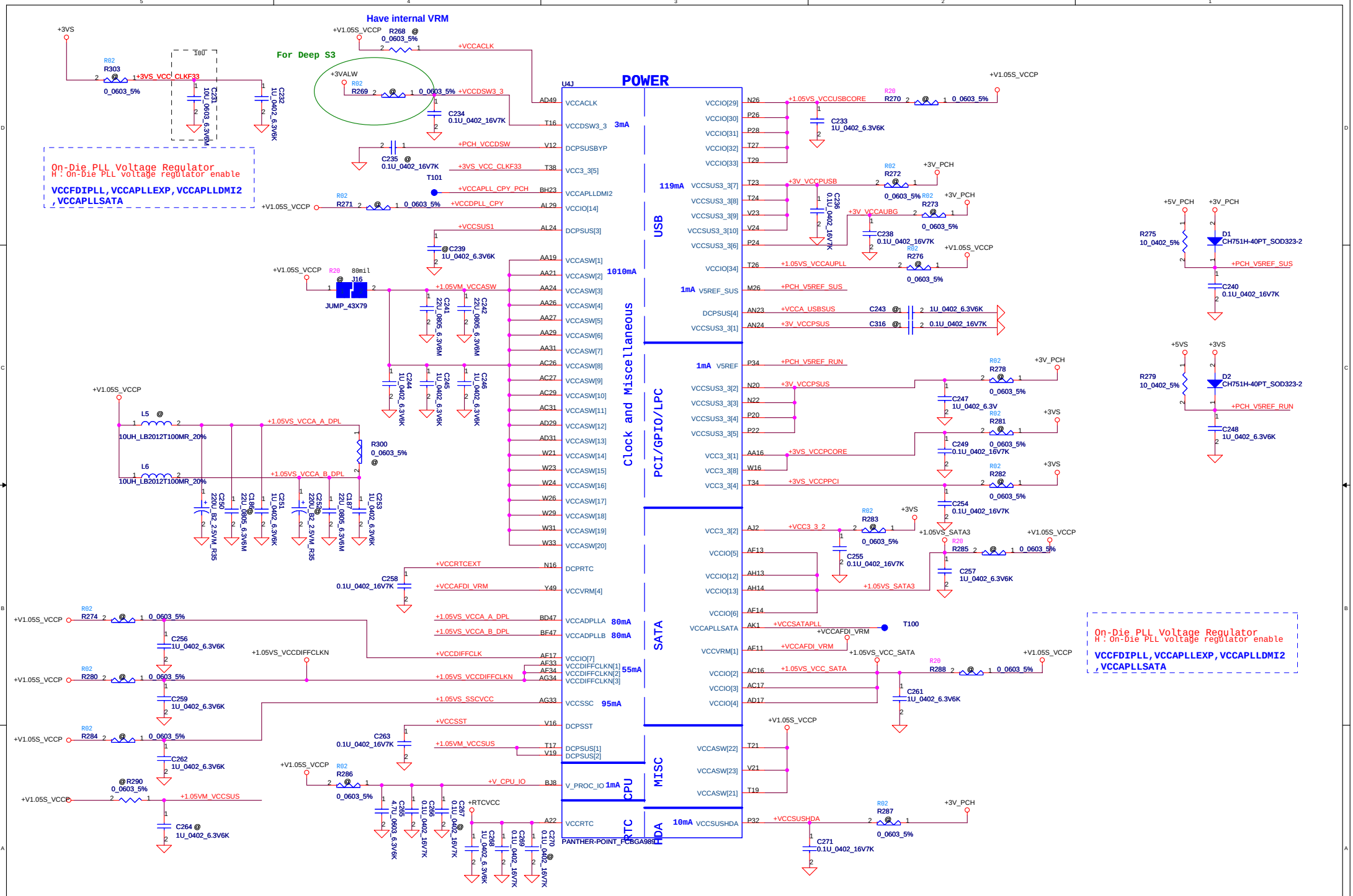

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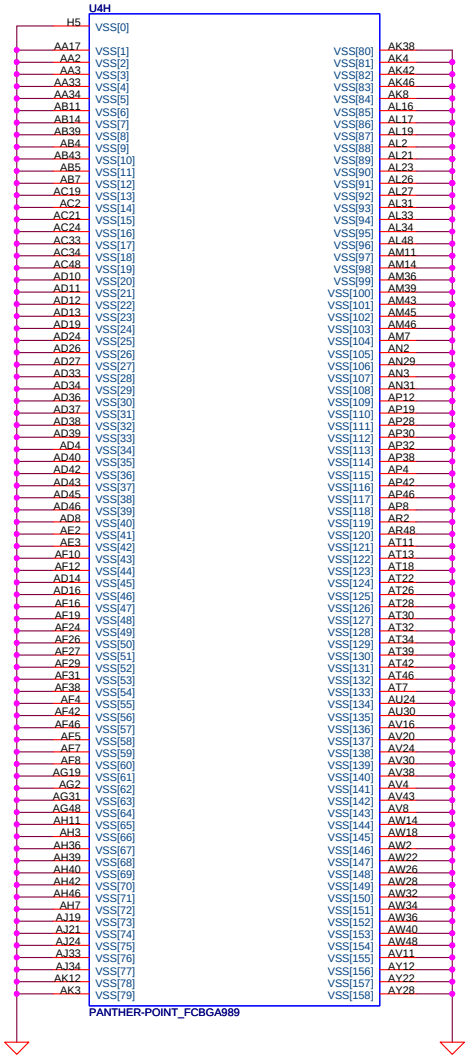

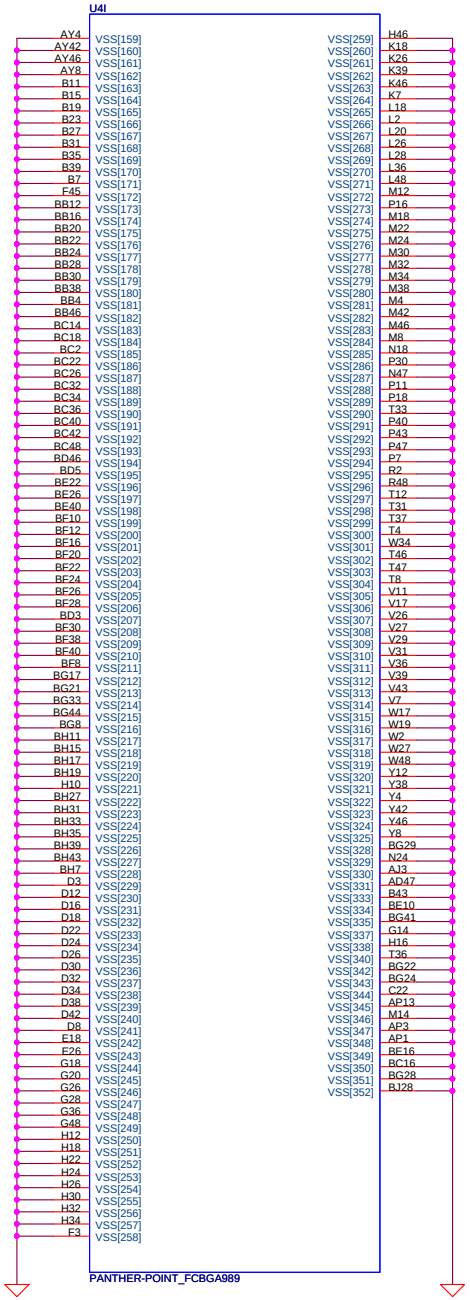

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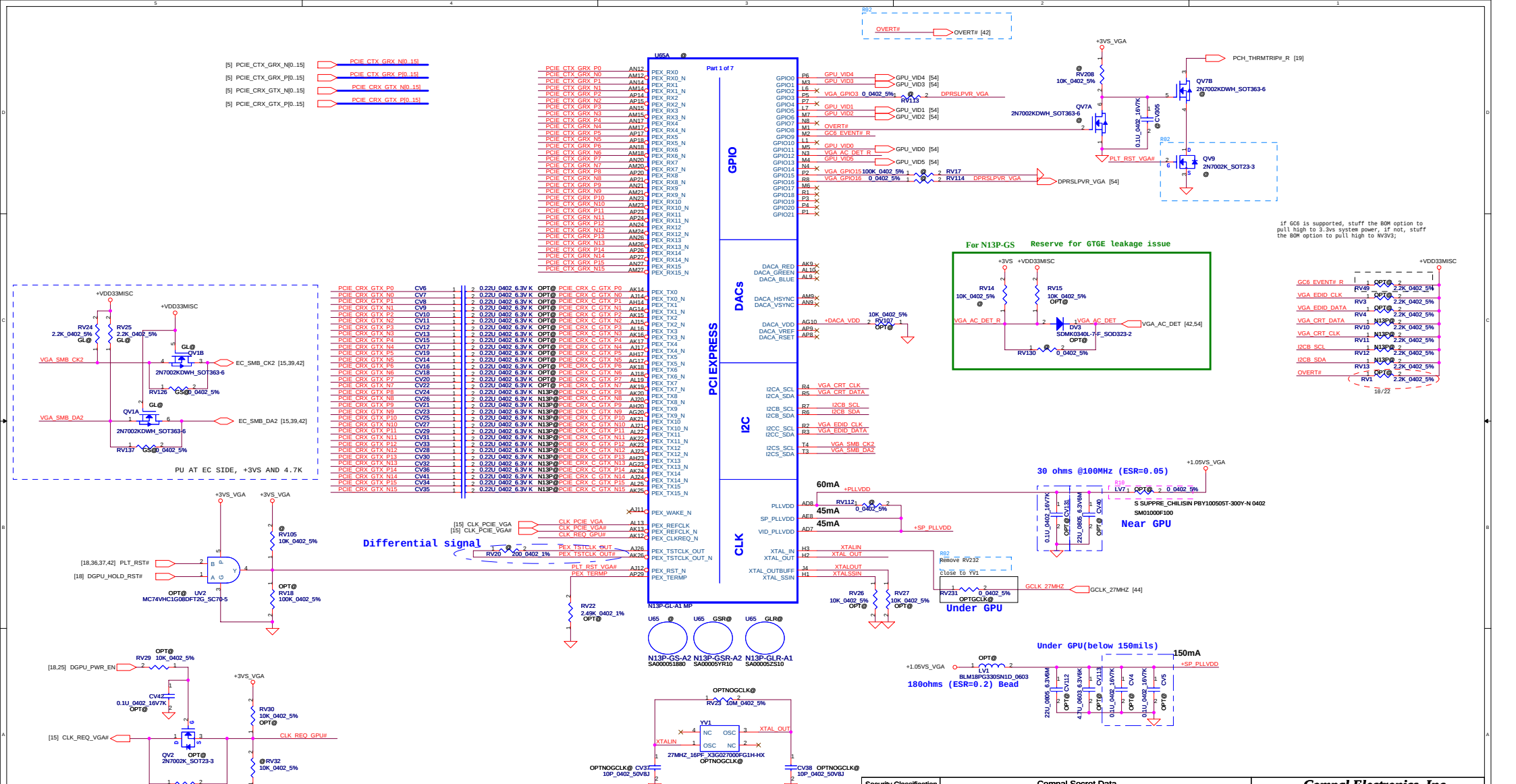

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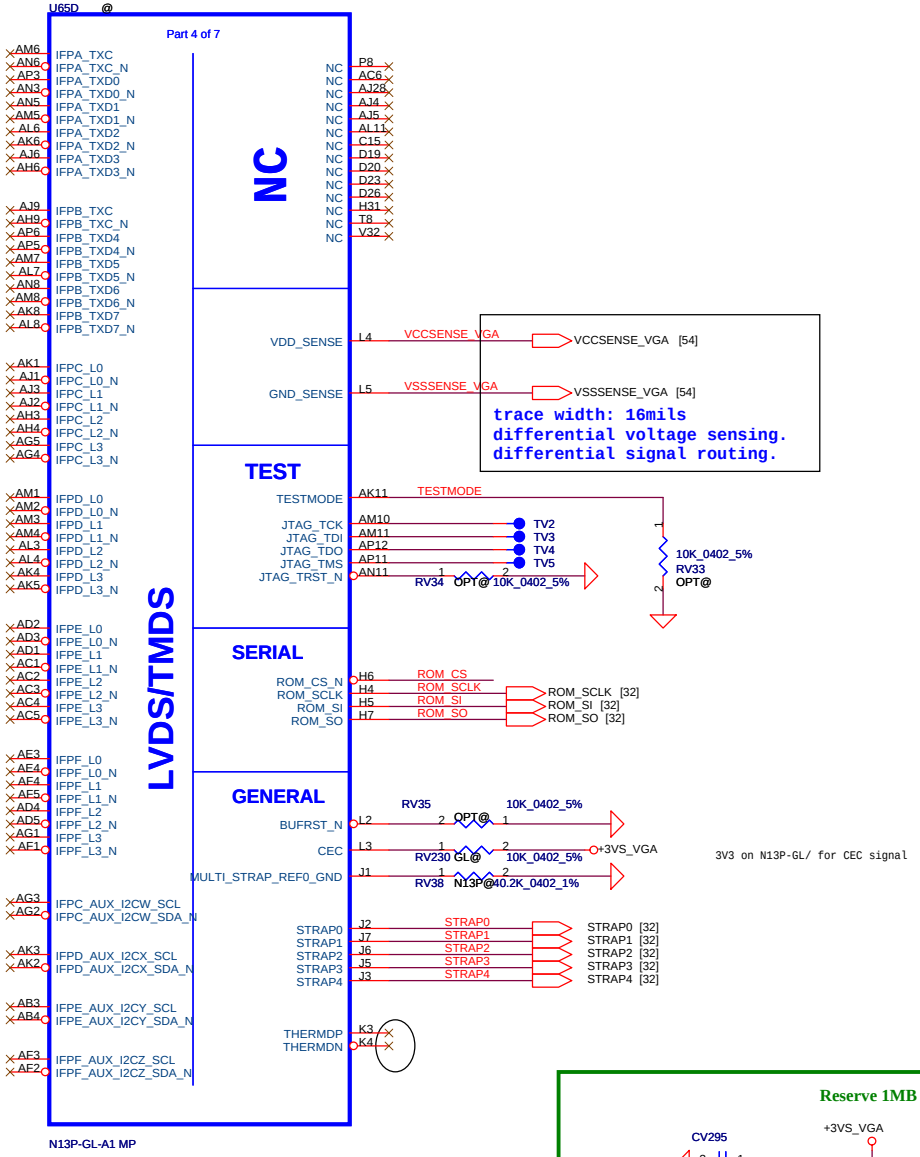

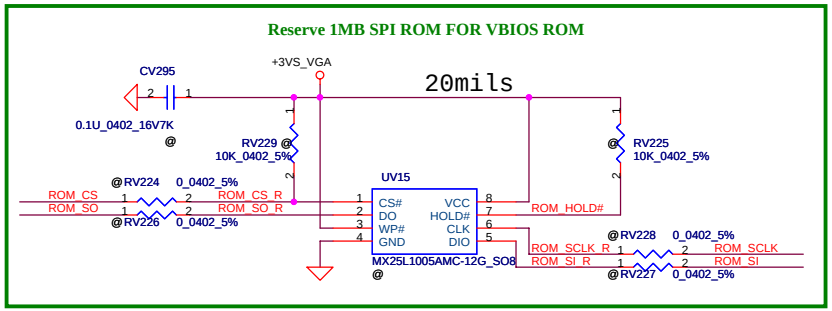

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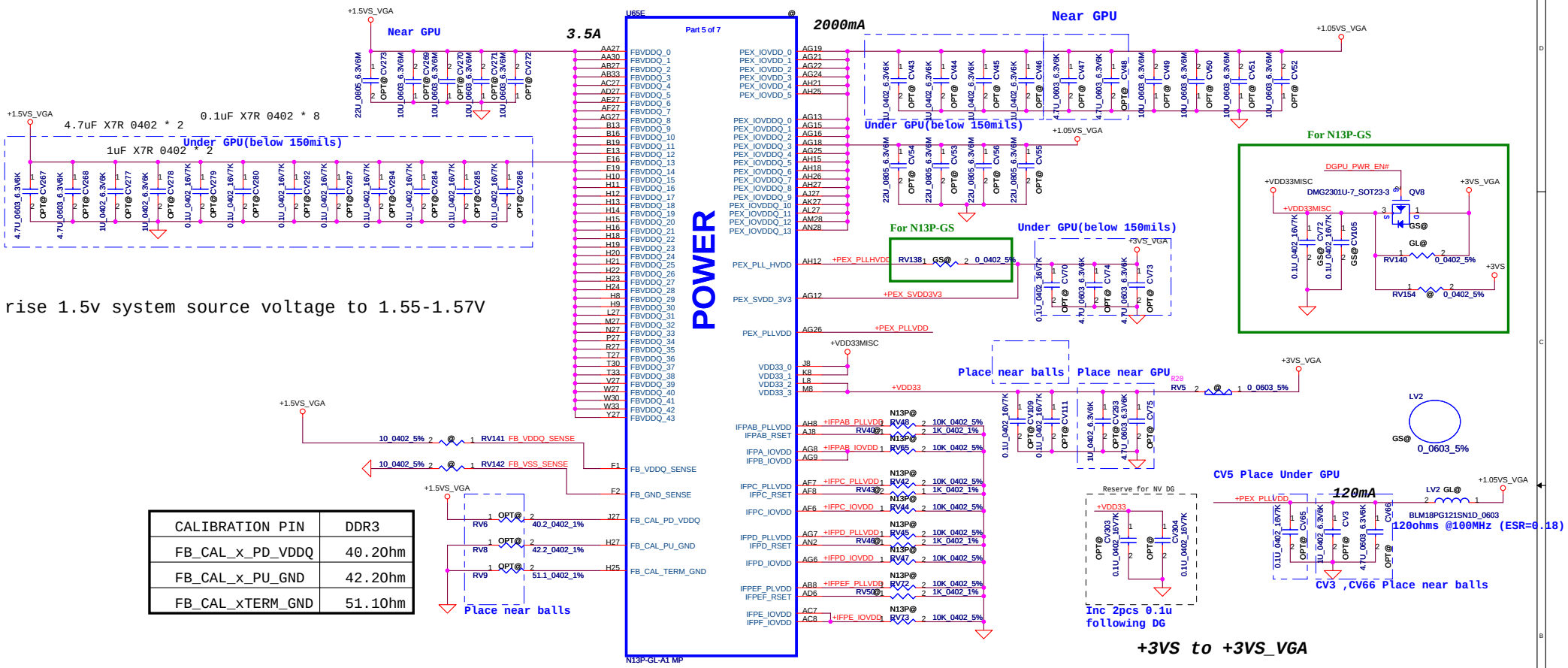

CALIBRATION PIN	DDR3
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	42.2Ohm
FB_CAL_xTERM_GND	51.1Ohm

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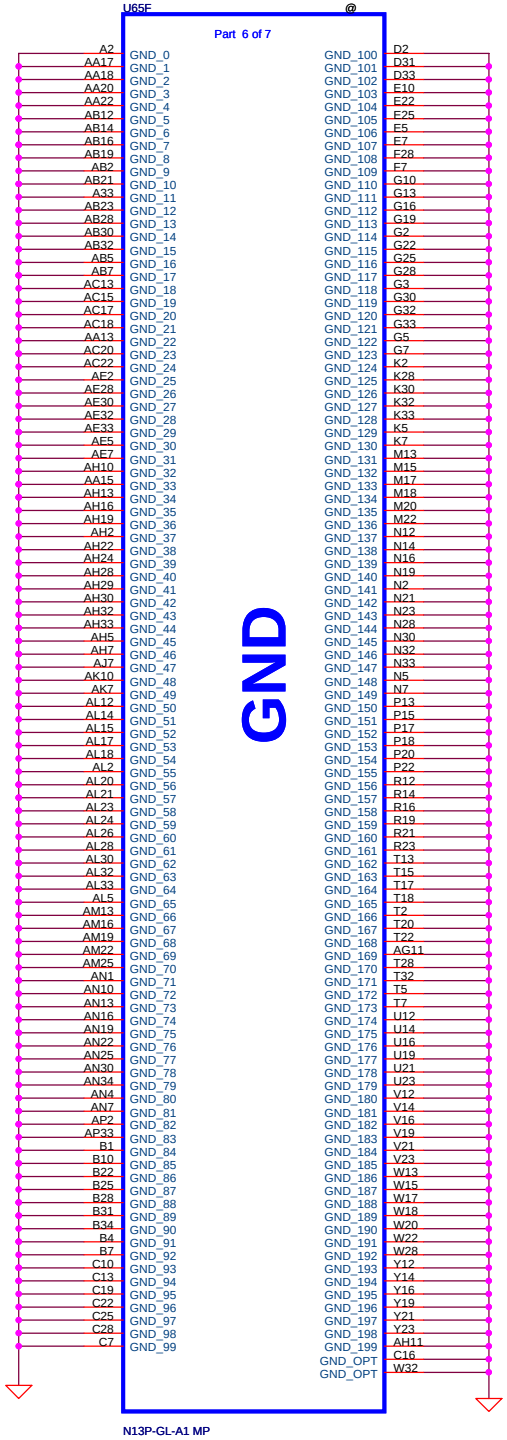

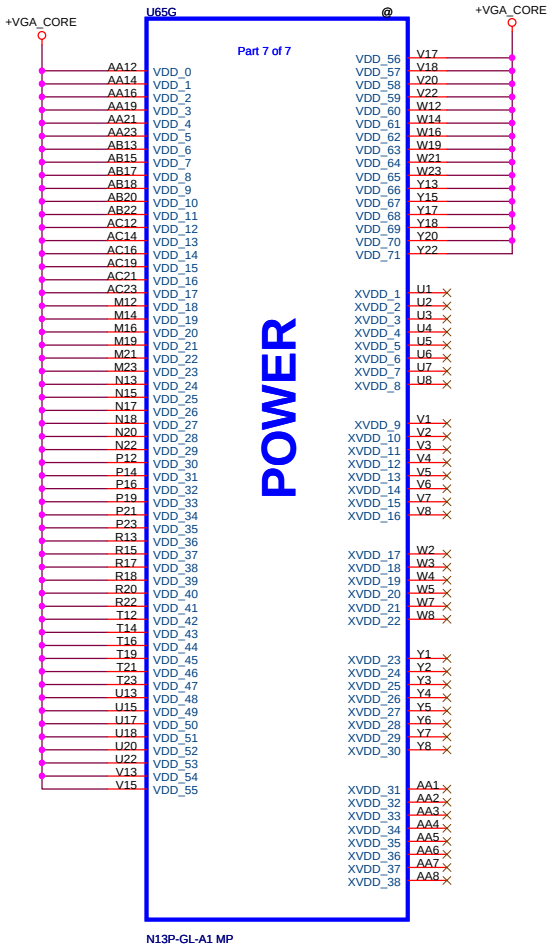

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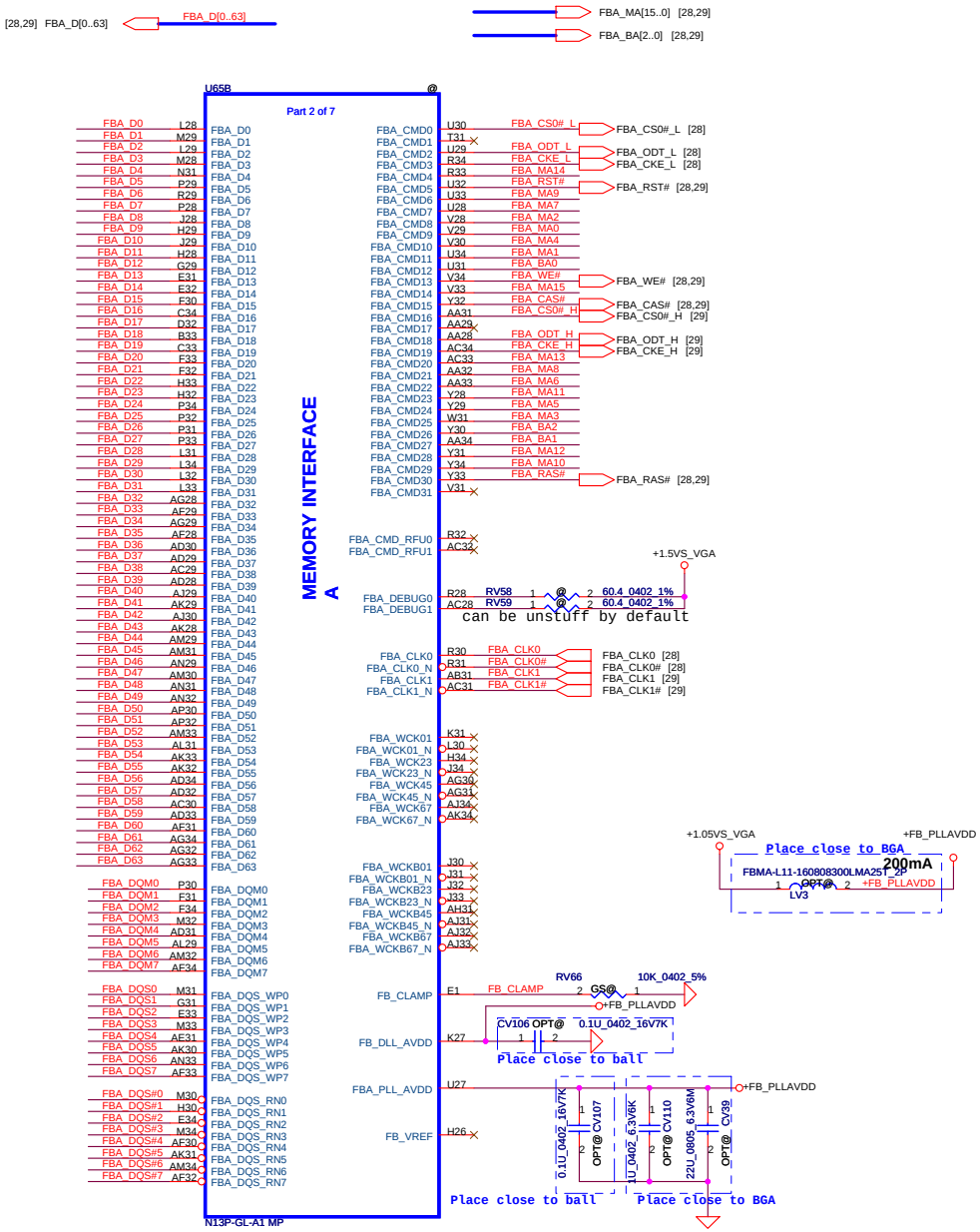

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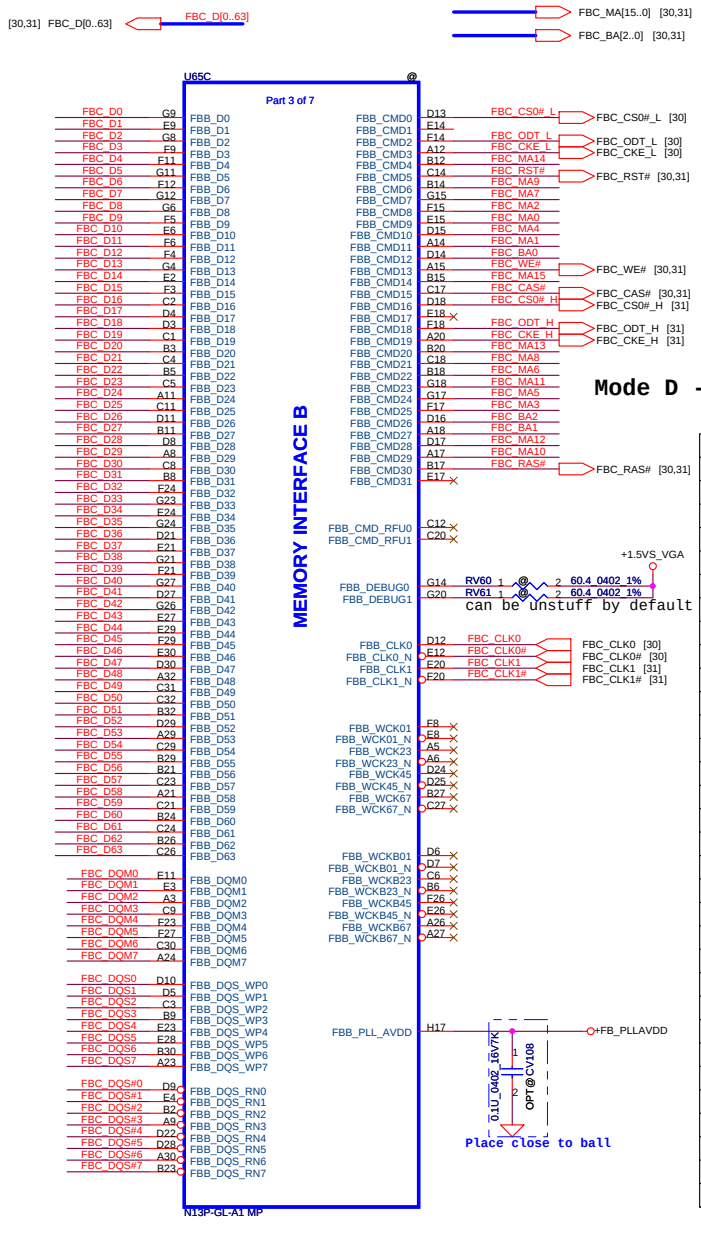

Mode D - Mirror Mode Mapping

Address	DATA Bus 0..31	DATA Bus 32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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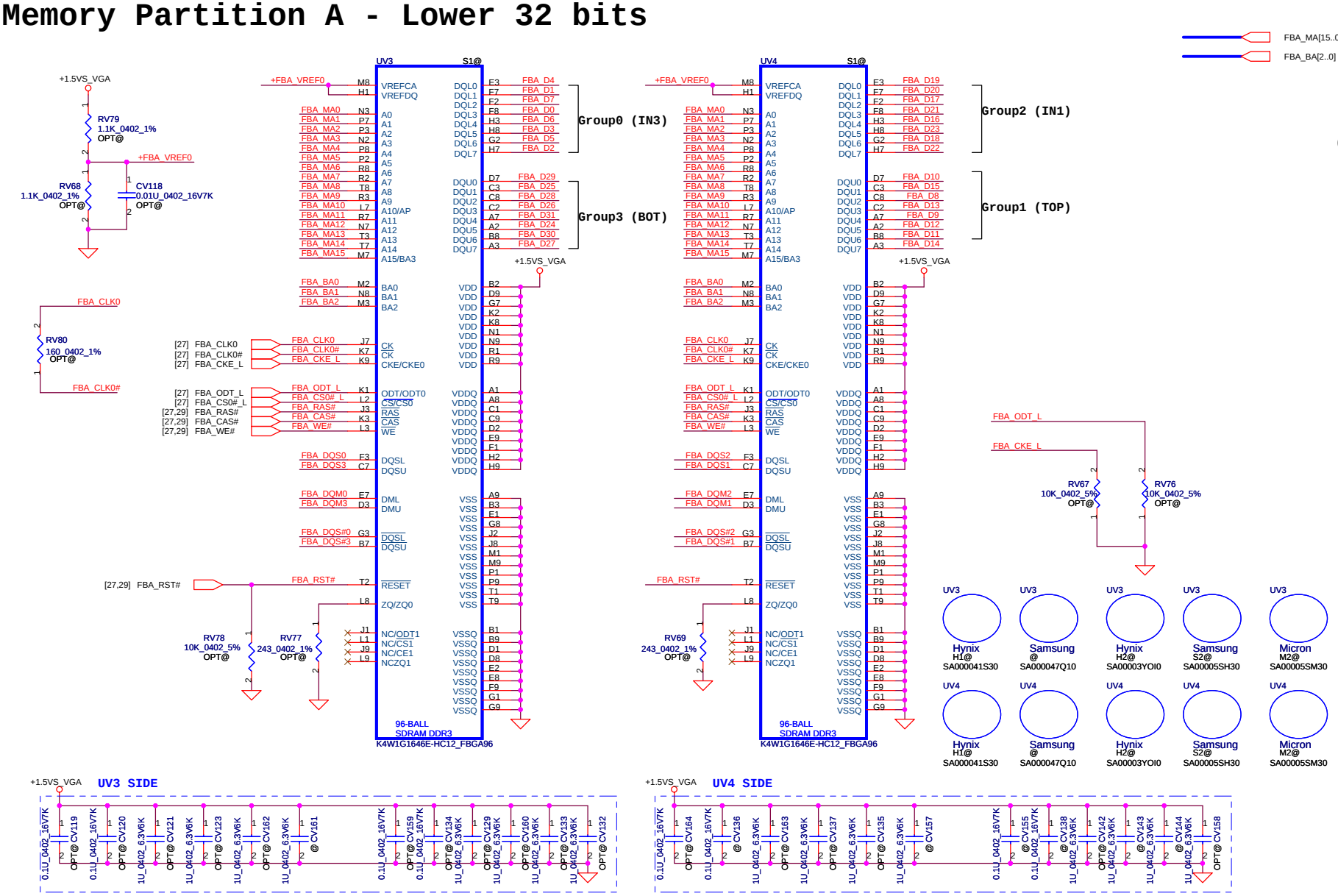
Memory Partition A - Lower 32 bits



FBA_D[0..63] [27,29]
FBA_MA[15..0] [27,29]
FBA_BA[2..0] [27,29]
FBA_DQM[7..0] [27,29]
FBA_DQS[7..0] [27,29]
FBA_DQS#[7..0] [27,29]

CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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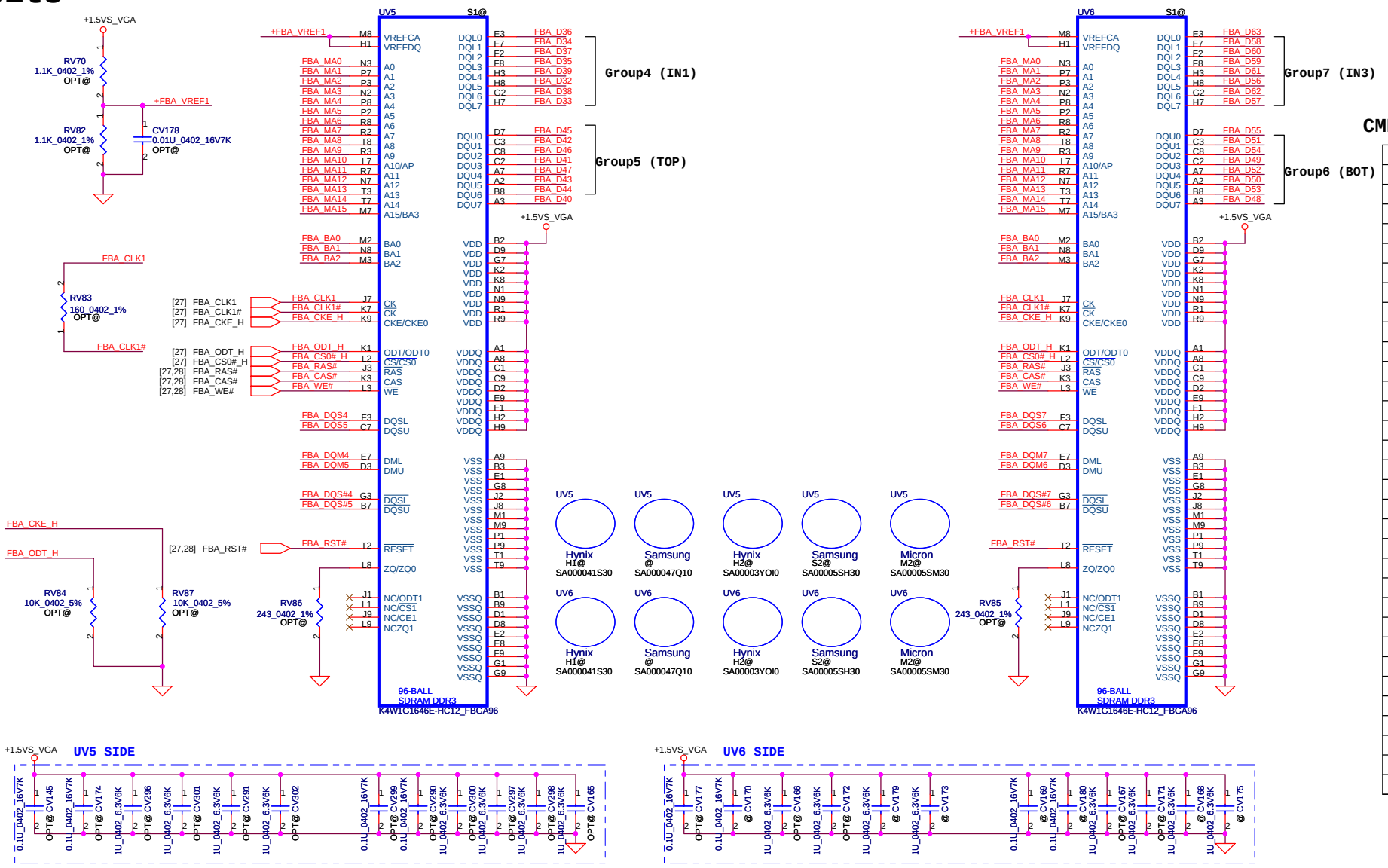
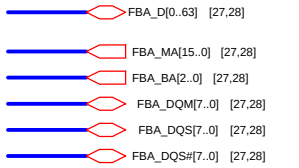
Memory Partition A - Upper 32 bits





CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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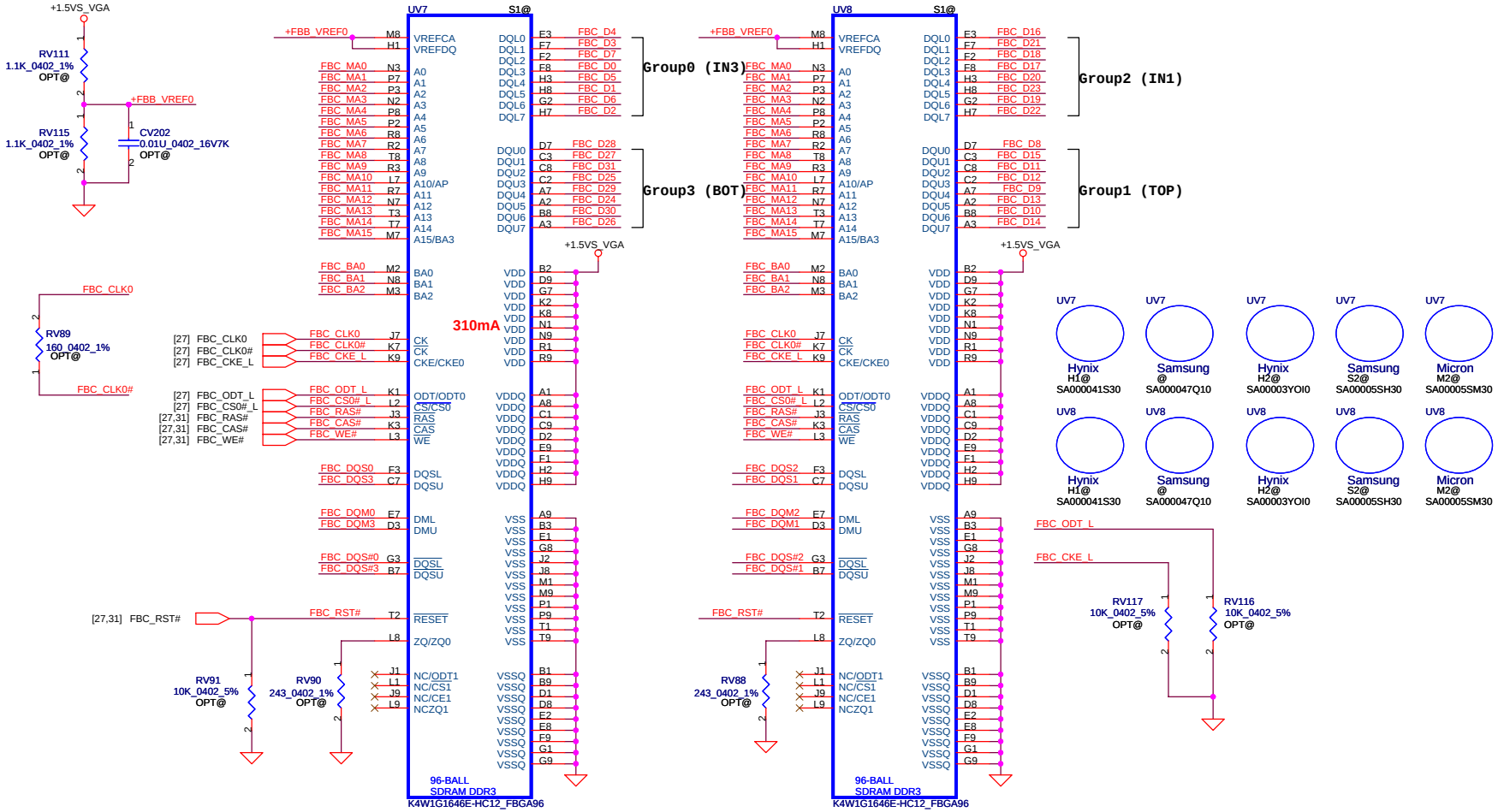
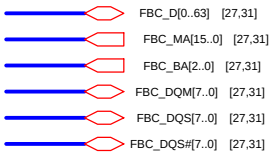
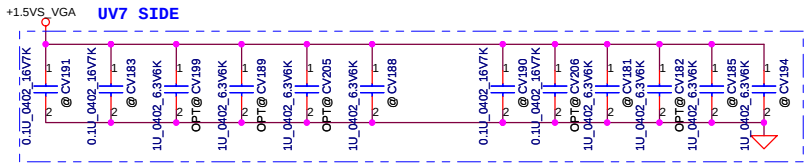
Memory Partition C - Lower 32 bits

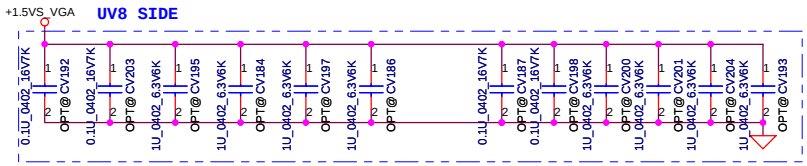




CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#





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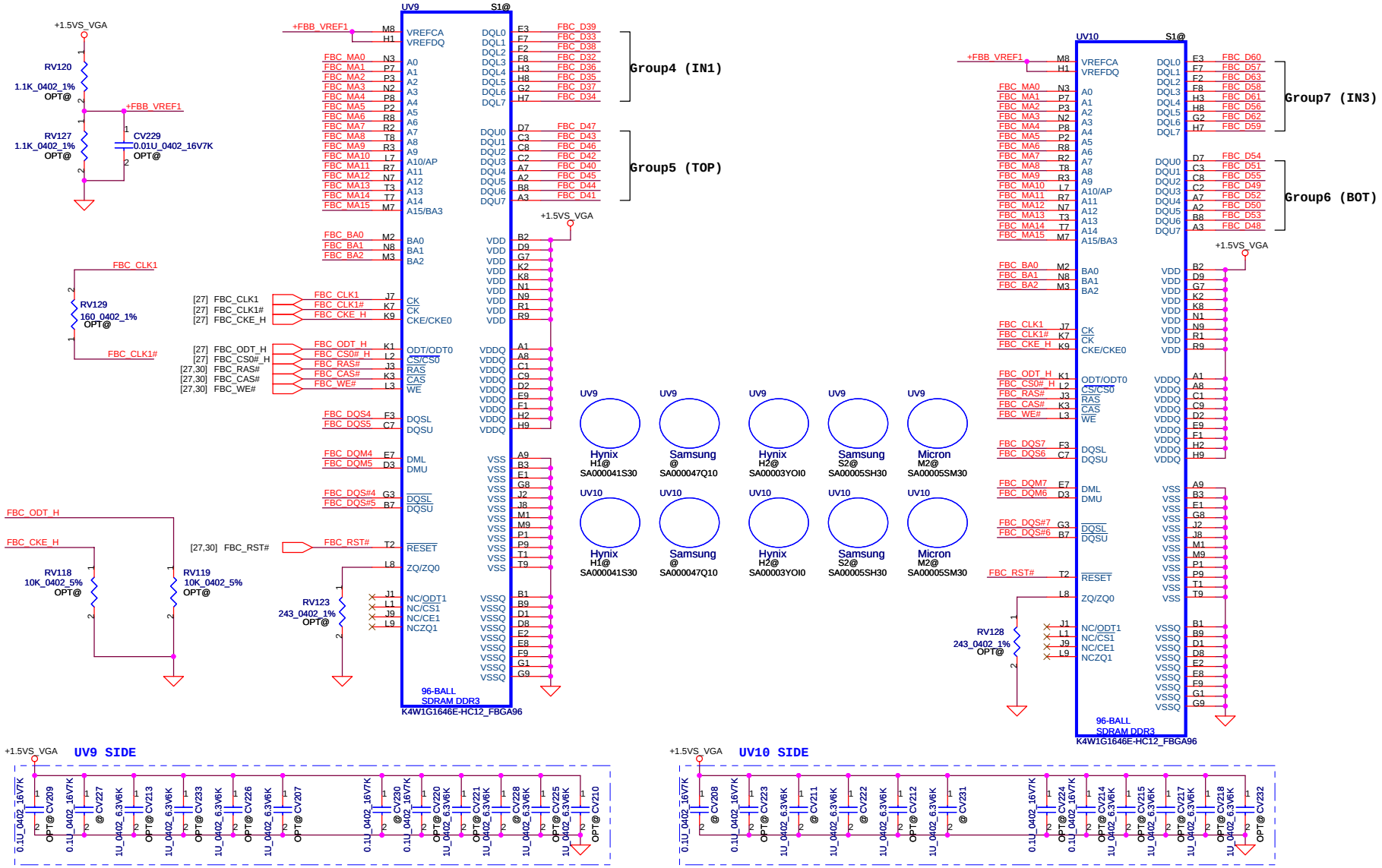
Memory Partition C - Upper 32 bits



CMD mapping mod Mode D

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

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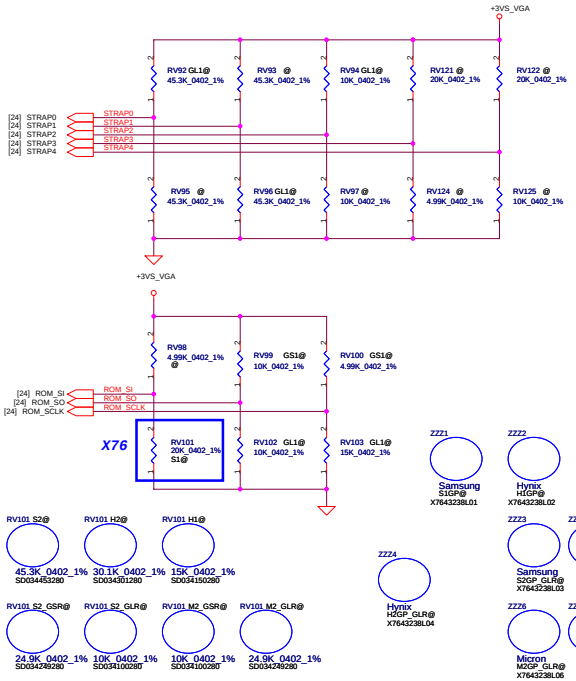

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG/PCI_DEVID[5]	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Vendor	VRAM Sturcture
Samsung 2G	S2@
Hynix 2G	H2@
Samsung 1G	S1@
Hynix 1G	H1@

SUB_VENDOR

0	No VBIOS ROM
1	BIOS ROM is present (Default)

3GIO_PADCFG

3GIO_PADCFG[3:0]	
0110	Notebook Default

XCLK_417

0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE

0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SLOT_CLK_CFG

0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR

0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE

0	3D Device (Class Code 302h)
1	VGA Device (Default)

USER Straps

User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM

0	Disable (Default)
1	Enable

PCIE_MAX_SPEED

0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

For N13P-GS strap table

X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 30.1K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 5K	R PD 15K	R PD 5K	R PD 45K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PU 5K	R PD 15K	R PD 5K	R PD 45K	R PD 15K	R PU 10K	R PU 5K

strap0 RV92 GS1@ 45.3K_0402_1% SD034453280
strap1 RV96 GS1@ 4.99K_0402_1% SD034499180
strap2 RV97 GS1@ 15K_0402_1% SD034150280
strap3 RV124 GS1@ 4.99K_0402_1% SD034499180
strap4 RV125 GS1@ 45.3K_0402_1% SD034453280

For N13P-GSR strap table

X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 5K	R PU 10K	R PD 5K	R PD 45K	R PD 45K	R PU 10K	R PU 5K
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 5K	R PU 10K	R PD 5K	R PD 45K	R PD 30.1K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 5K	R PU 10K	R PD 5K	R PD 45K	R PD 20K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PU 5K	R PU 10K	R PD 5K	R PD 45K	R PD 15K	R PU 10K	R PU 5K

strap0 RV92_GSR@ 45.3K_0402_1% SD034453280
strap1 RV96_GSR@ 4.99K_0402_1% SD034499180
strap2 RV94_GSR@ 10K_0402_1% SD034100280
strap3 RV124 GSR@ 4.99K_0402_1% SD034499180
strap4 RV125 GSR@ 45.3K_0402_1% SD034453280
ROM_SO RV99_GSR@ 10K_0402_1% SD034100280
ROM_SCLK RV100 GSR@ 4.99K_0402_1% SD034499180

For N13P-GL strap table

X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 30.1K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

For N13P-GLR strap table

X76

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GL	900 MHz	128M* 16* 8 2GB	Samsung (2Gb) K4W2G1646C-HC11	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 45K	R PD 10K	R PD 15K
N13P-GL	900 MHz	128M* 16* 8 2GB	Hynix (2Gb) H5TQ2G63DFR-11C	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 30.1K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Samsung (1Gb) K4W1G1646G-BC11	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 20K	R PD 10K	R PD 15K
N13P-GL	900 MHz	64M* 16* 8 1GB	Hynix (1Gb) H5TQ1G63DFR-11C	R PU 45K	R PD 45K	R PD 20K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

strap0 RV92_GLR@ 45.3K_0402_1% SD034453280
strap1 RV96_GLR@ 45.3K_0402_1% SD034453280
strap2 RV97_GLR@ 20K_0402_1% SD034200280
strap3
strap4
ROM_SO RV102 GLR@ 10K_0402_1% SD034100280
ROM_SCLK RV103 GLR@ 15K_0402_1% SD034150280

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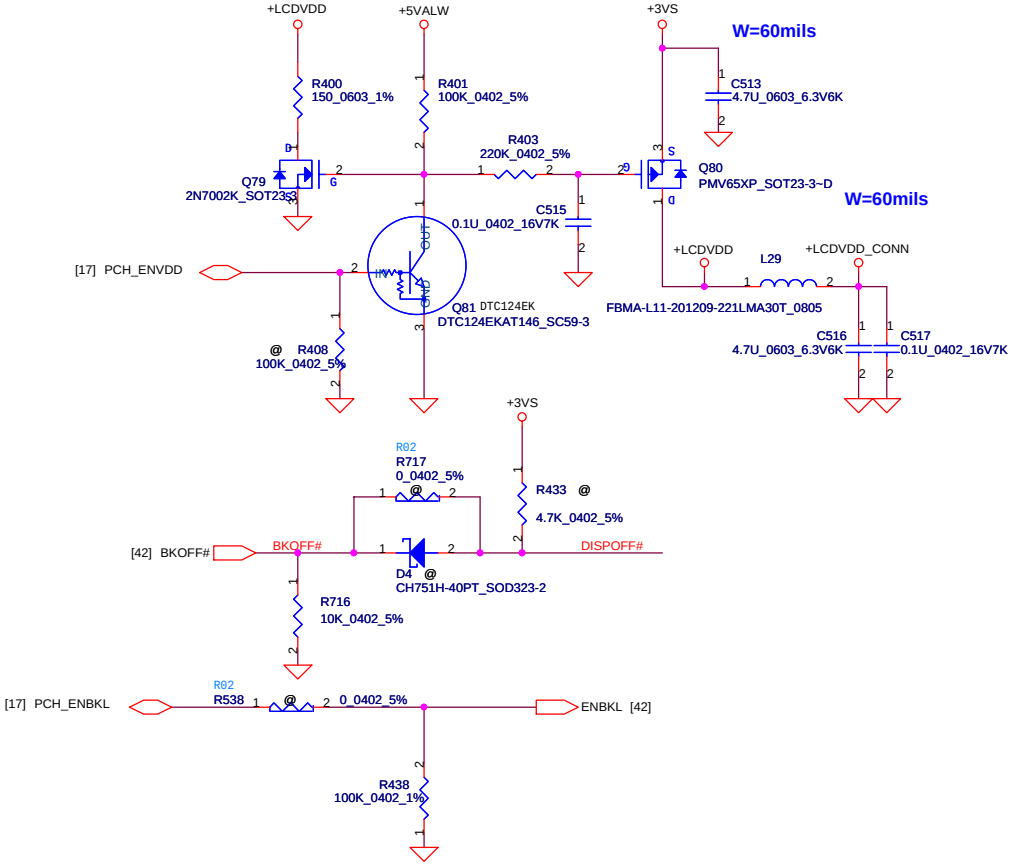
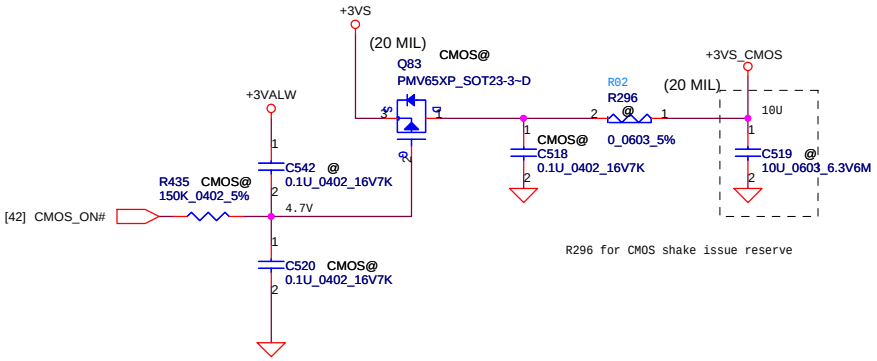
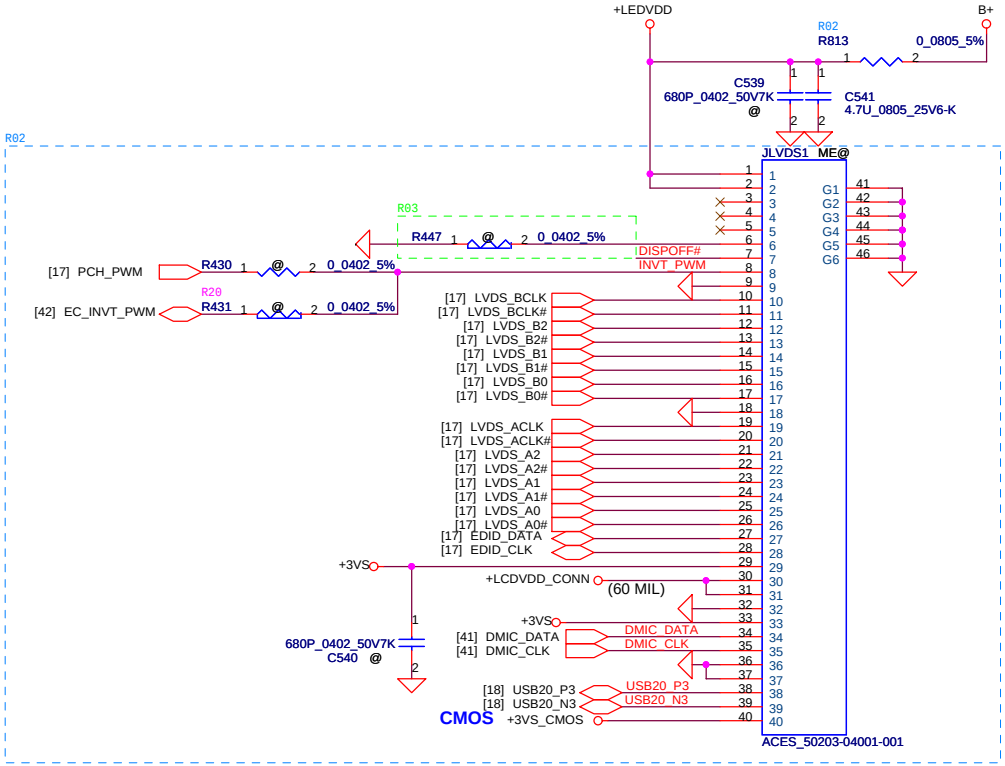
LCD POWER CIRCUIT



CMOS Camera



VGA LCD/PANEL BD. Conn.



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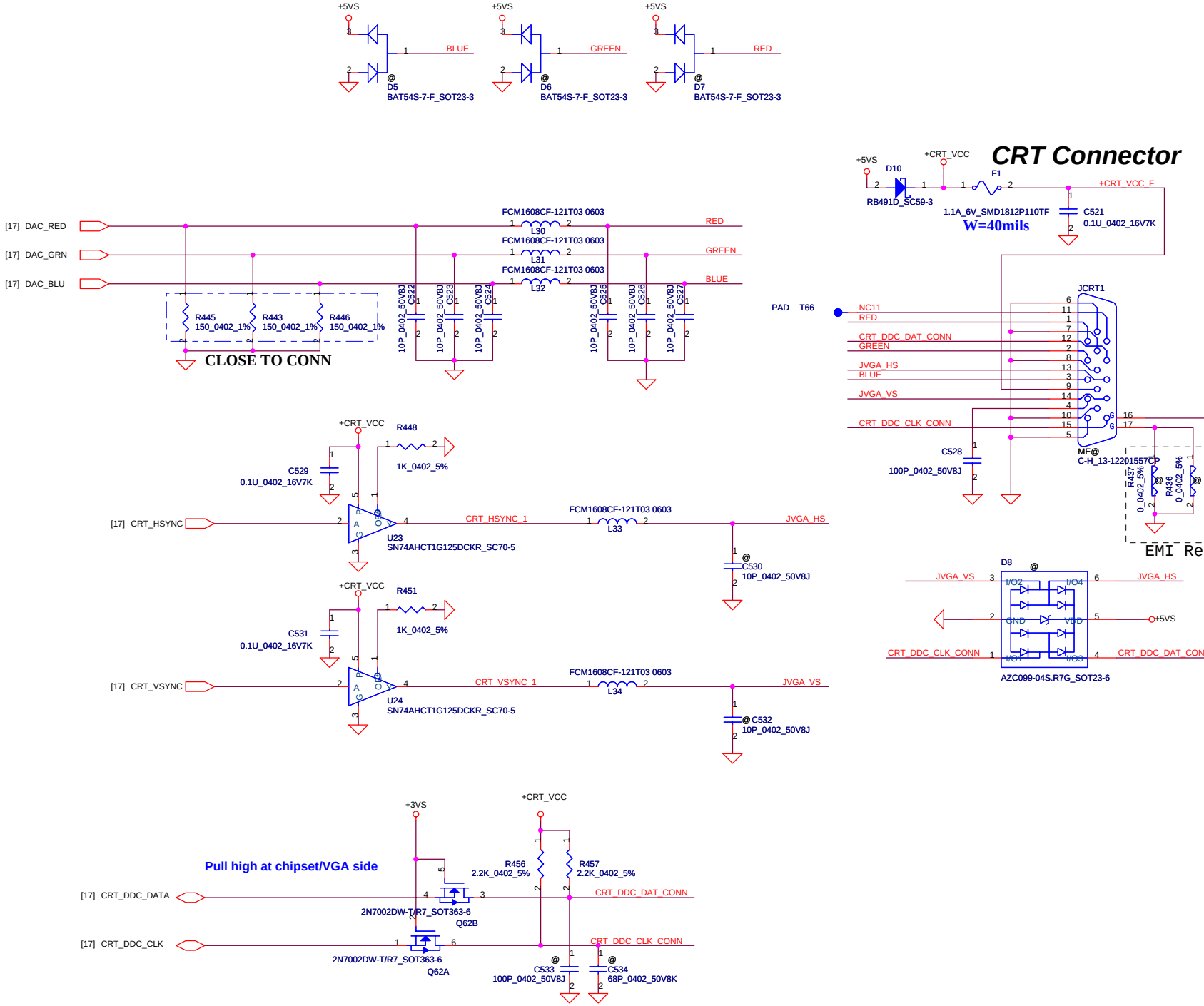

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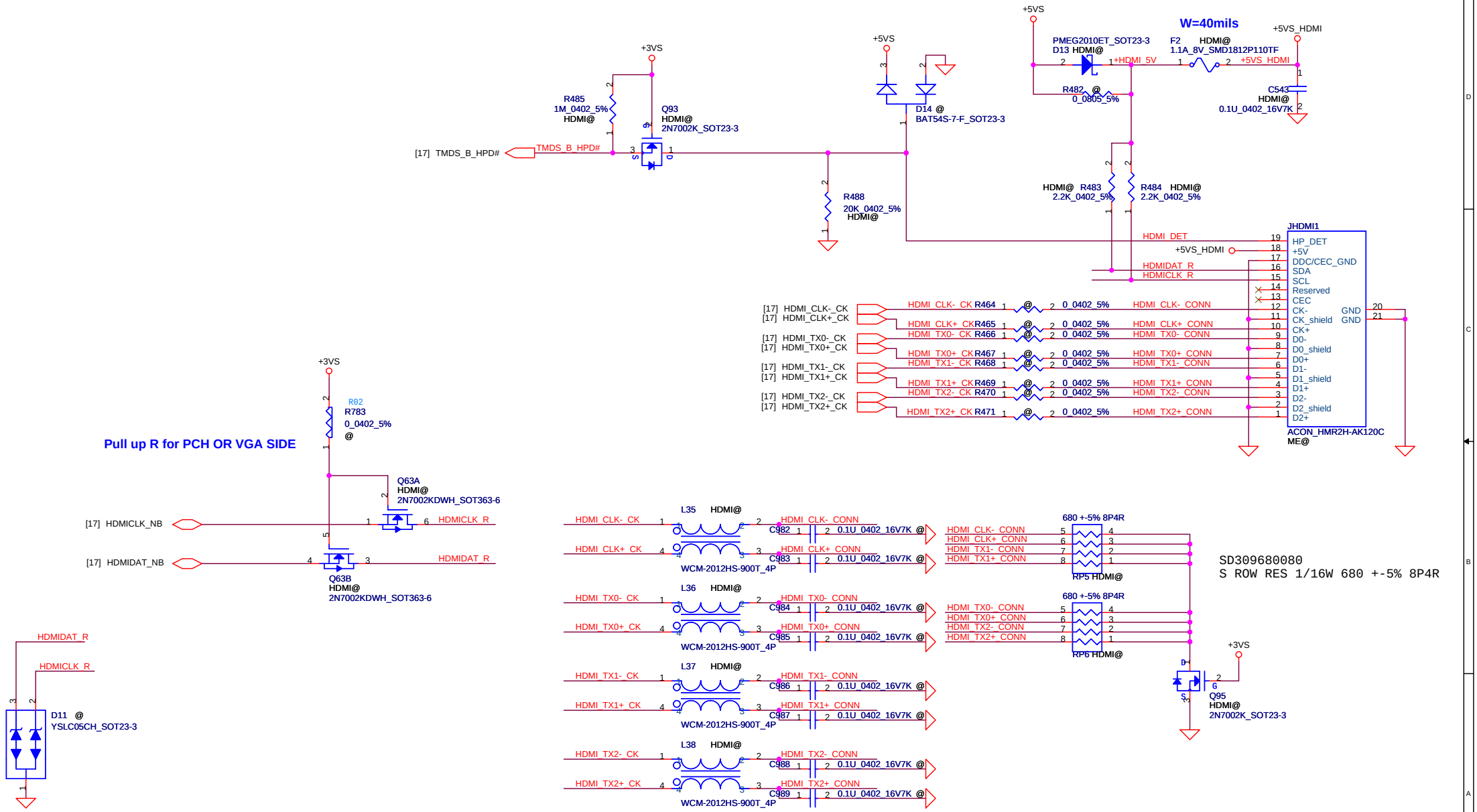

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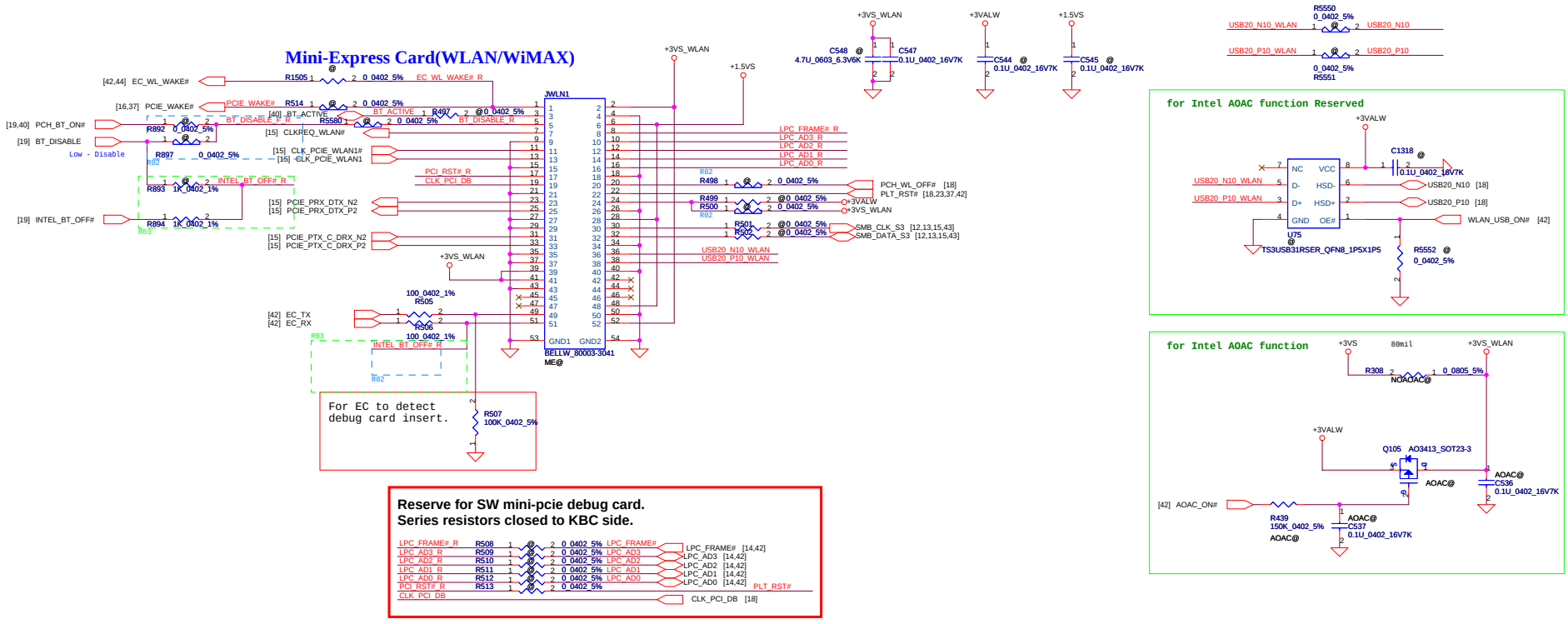
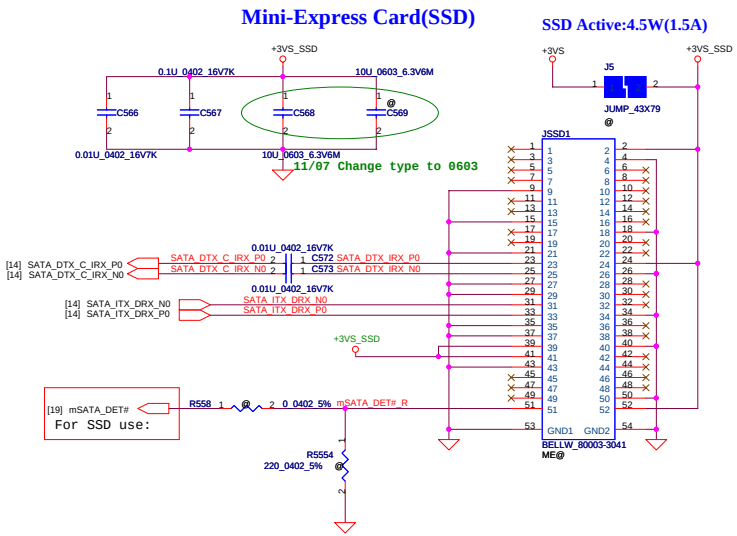
Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME#_R	R508	0_0402_5%	LPC_FRAME#	LPC_FRAME# [14,42]
LPC_AD3_R	R509	0_0402_5%	LPC_AD3	LPC_AD3 [14,42]
LPC_AD2_R	R510	0_0402_5%	LPC_AD2	LPC_AD2 [14,42]
LPC_AD1_R	R511	0_0402_5%	LPC_AD1	LPC_AD1 [14,42]
LPC_AD0_R	R512	0_0402_5%	LPC_AD0	LPC_AD0 [14,42]
PCI_RST#_R	R513	0_0402_5%		PLT_RST#
CLK_PCI_DB				CLK_PCI_DB [18]



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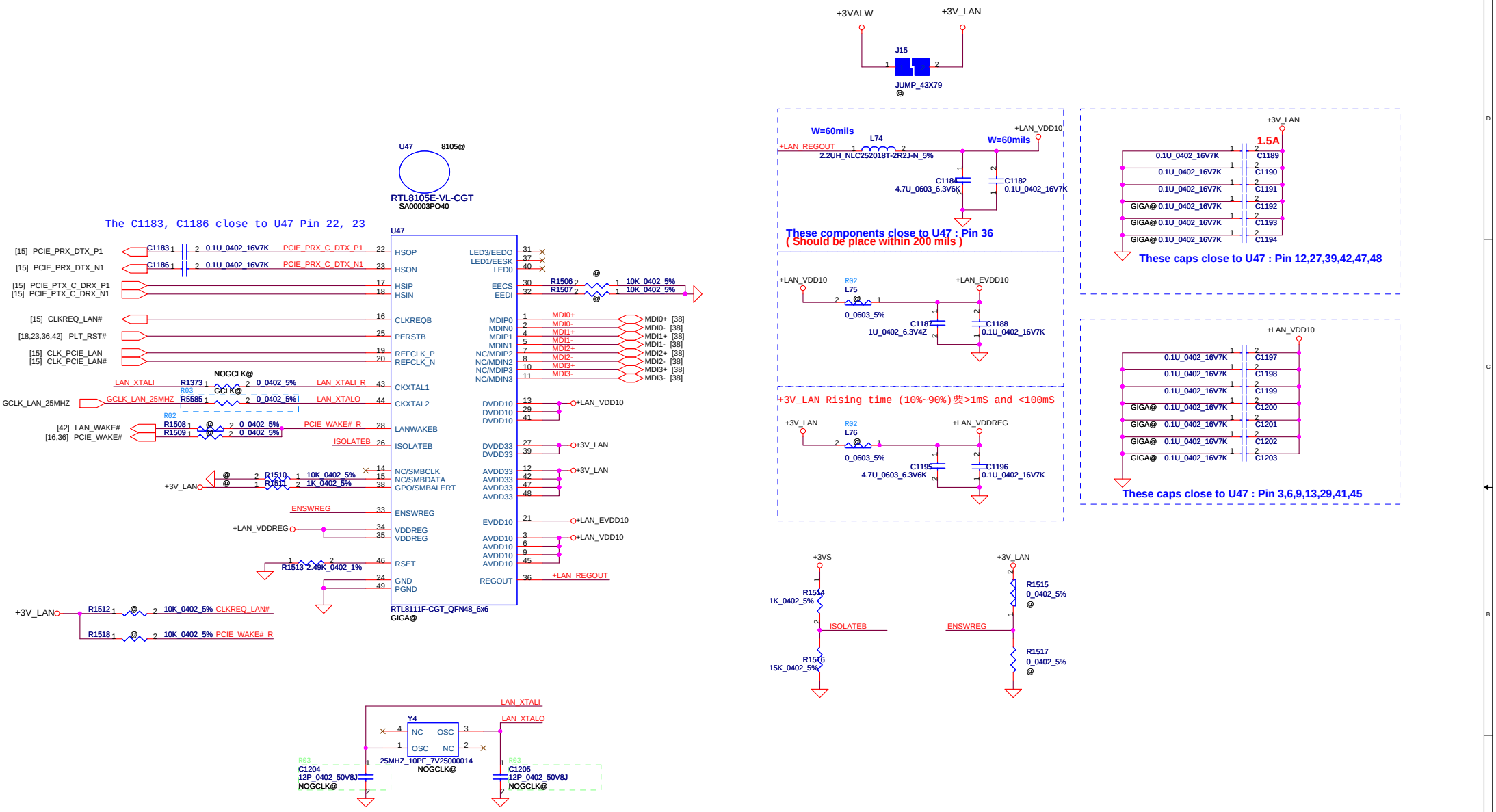

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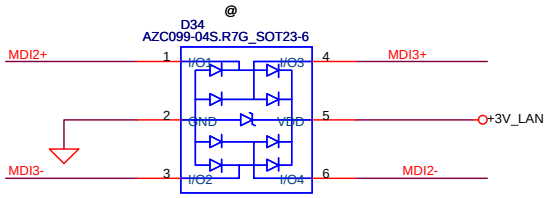
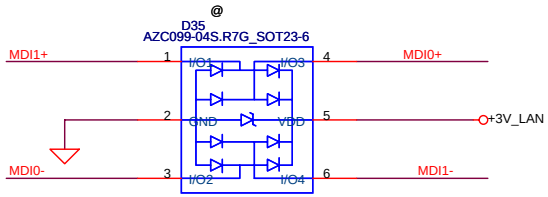


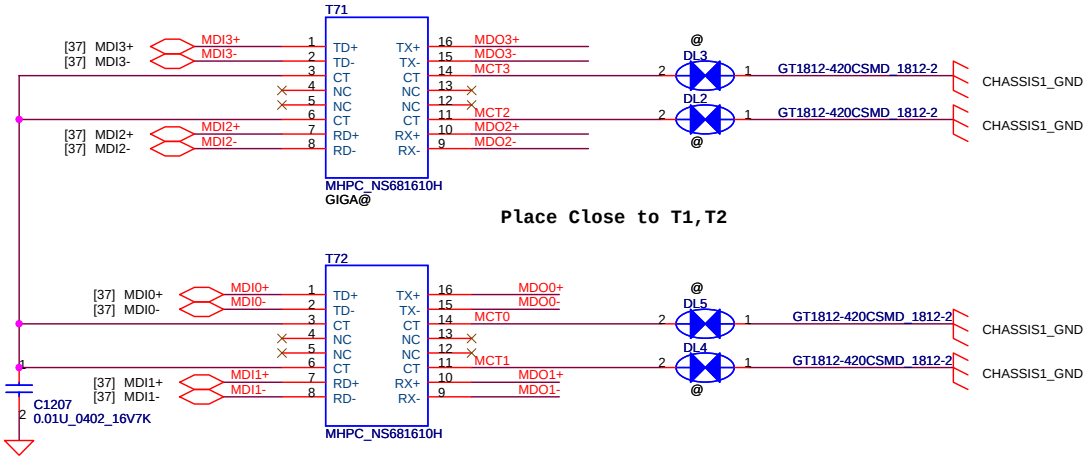
Place Close to T71



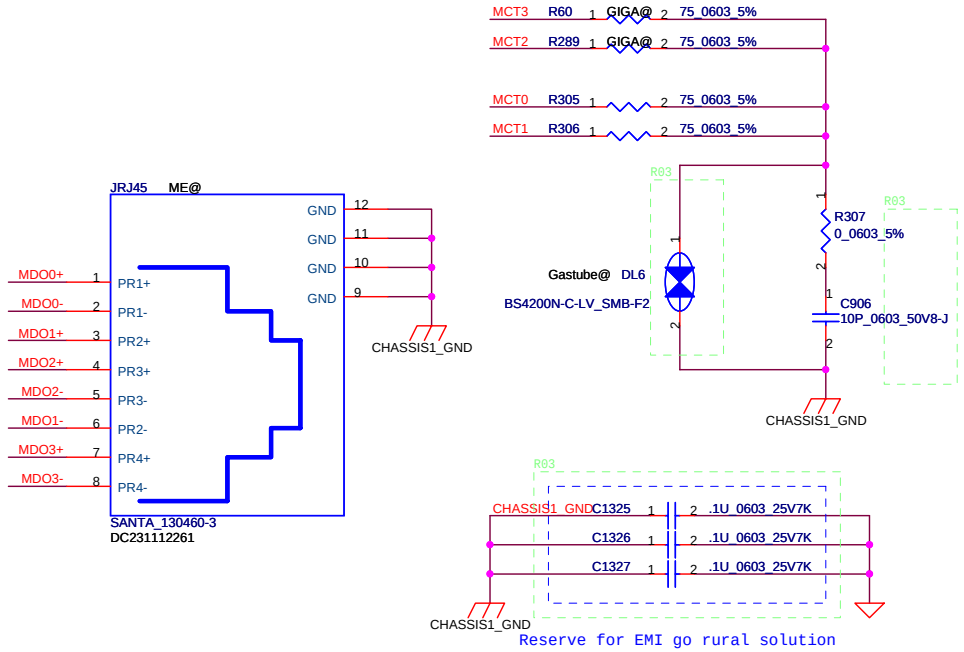
Place Close to T72

D34/D35
1'S PN:SC300001G00
2'S PN:SC300002E00

Reserve gas tube for EMI go rural solution



Place Close to T1,T2



Reserve for EMI go rural solution

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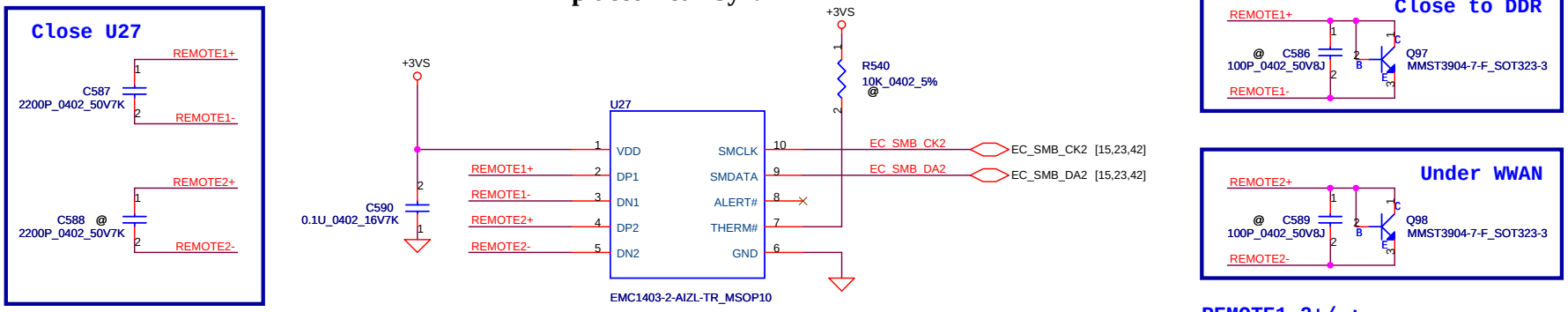
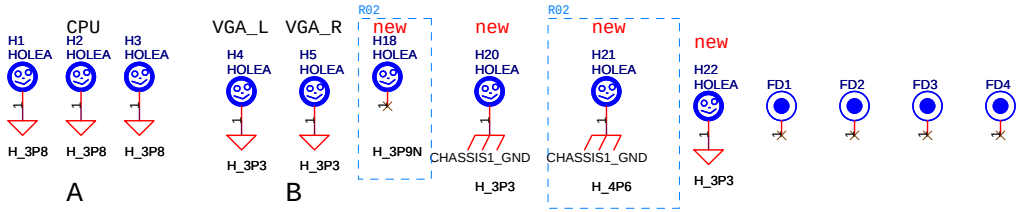
SMSC thermal sensor placed near by VRAM

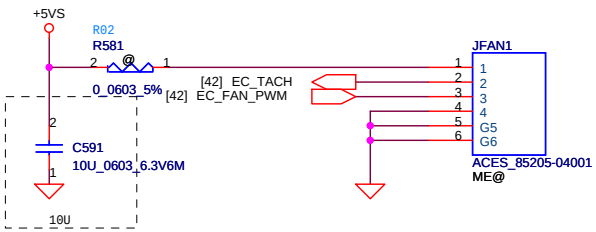


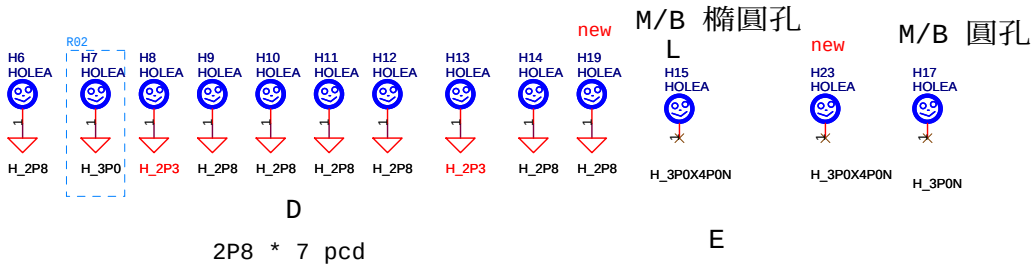
Address 1001_101xb

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



FAN1 Conn





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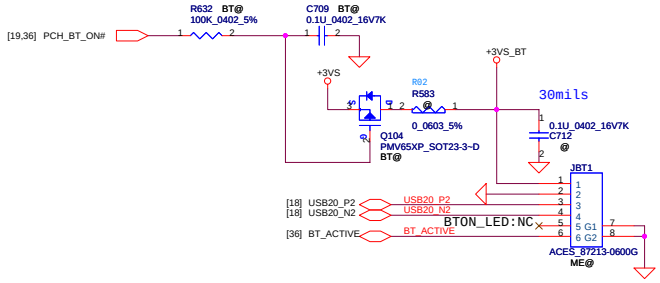
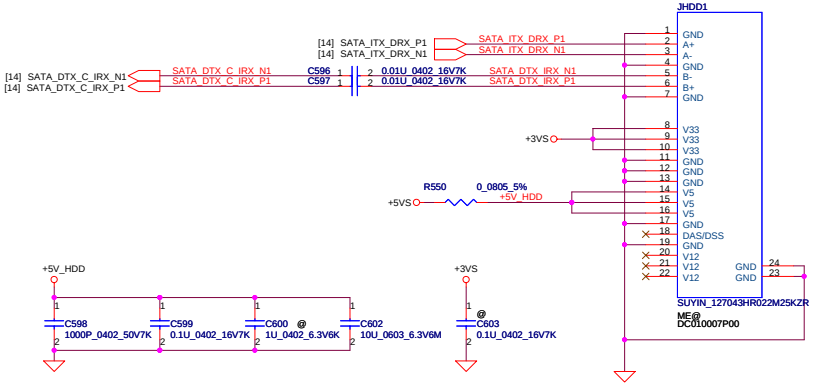
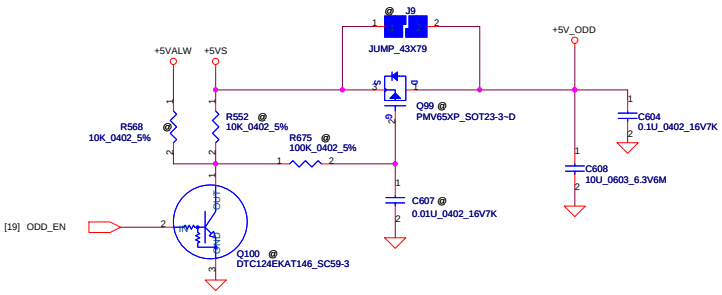
BT MODULE CONN



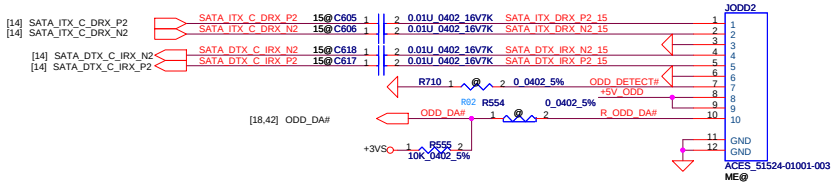
SATA HDD Conn.

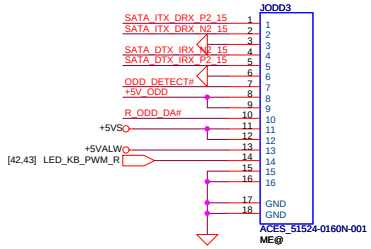


ODD Power Control



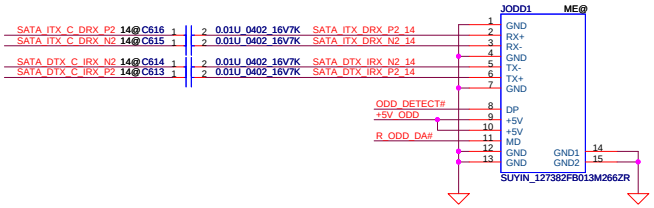
FOR 15" SATA ODD FFC Conn.





Co-lay

FOR 14" SATA ODD Conn.



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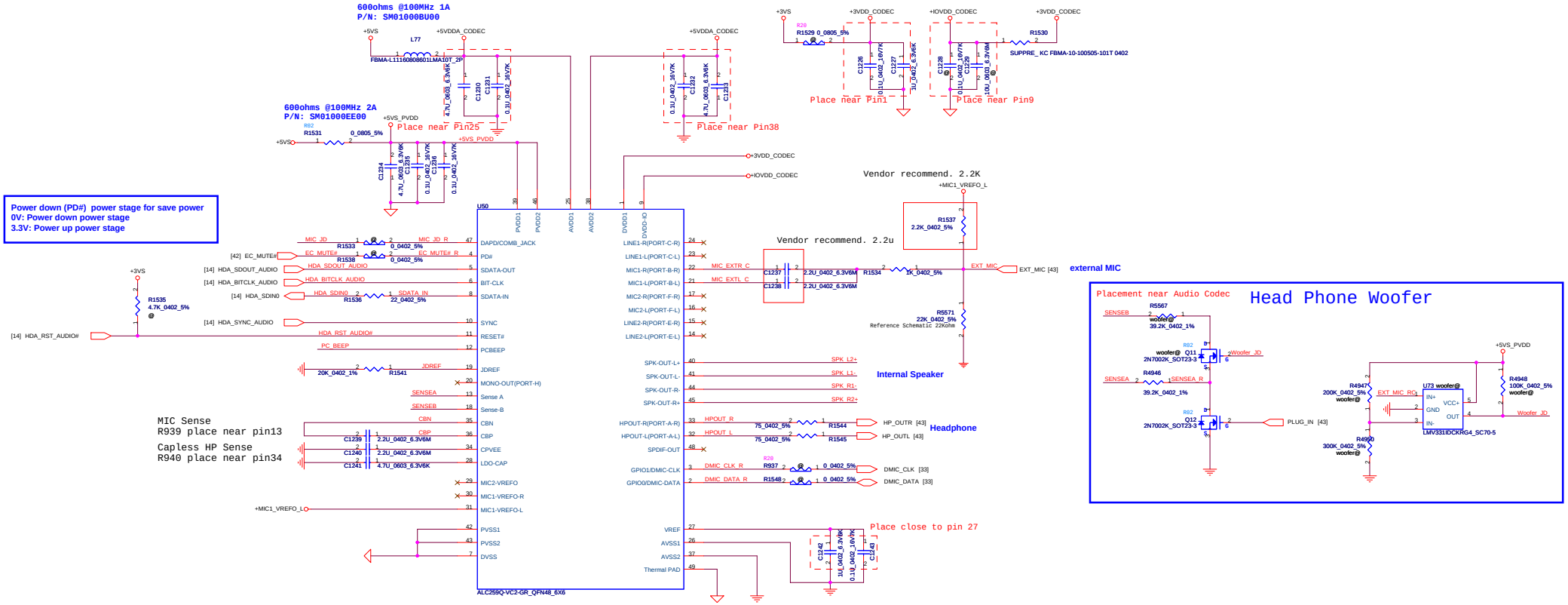
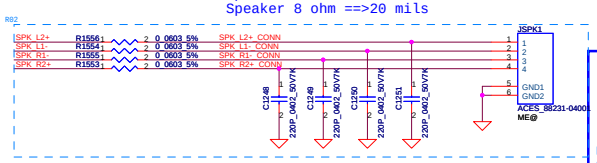
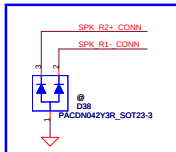


Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

wide 25MIL

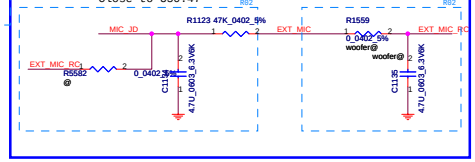
SPK L+L-R+R- trace width
Speaker 4 ohm ==>40 mils
Speaker 8 ohm ==>20 mils



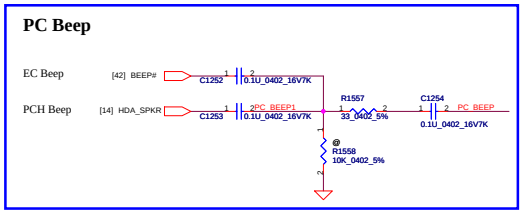


Reserve for ESD request.

Combo Jack detect (normal open)



PC Beep



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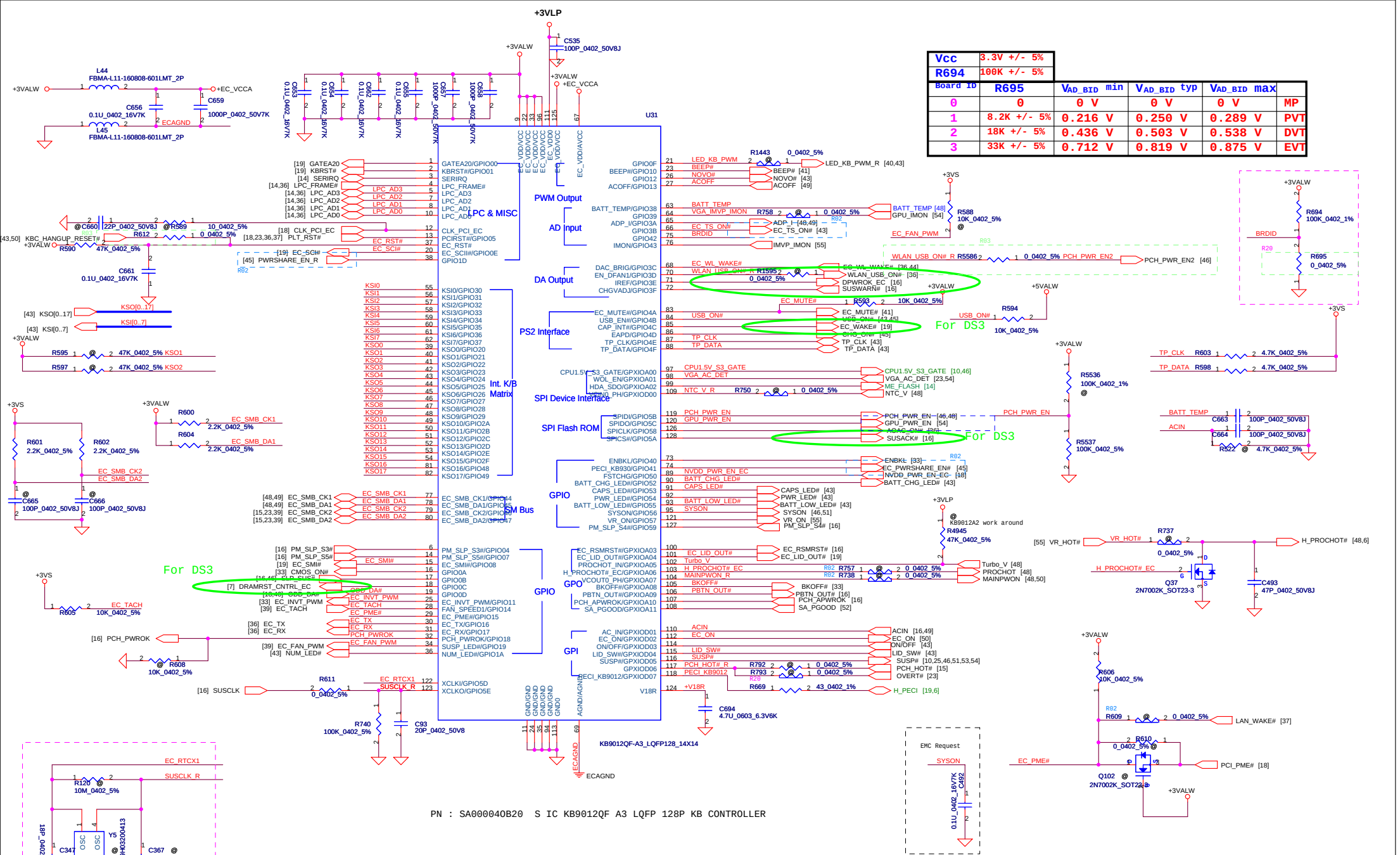

Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	VAD_BID min	VAD_BID typ	VAD_BID max	
0	0	0 V	0 V	0 V	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT

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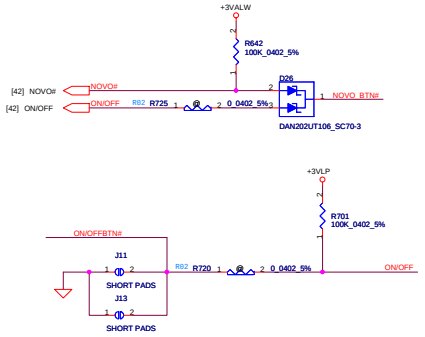
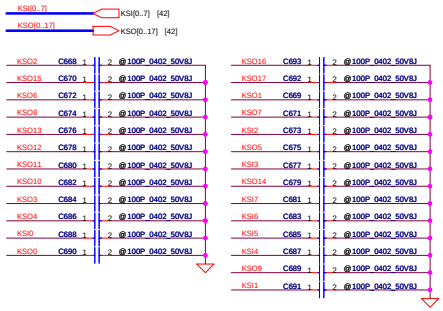
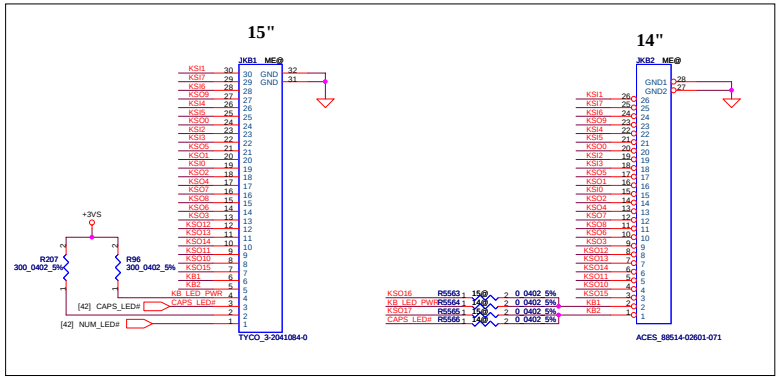
ON/OFF switch

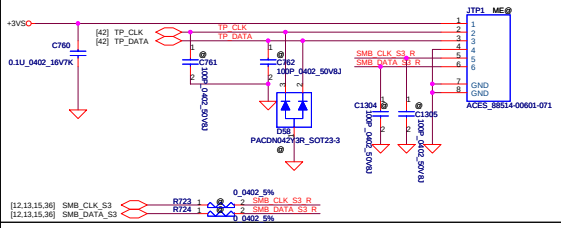


K/B Connector

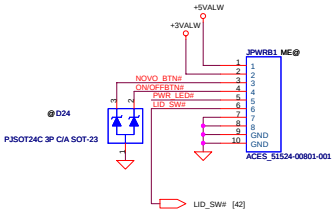




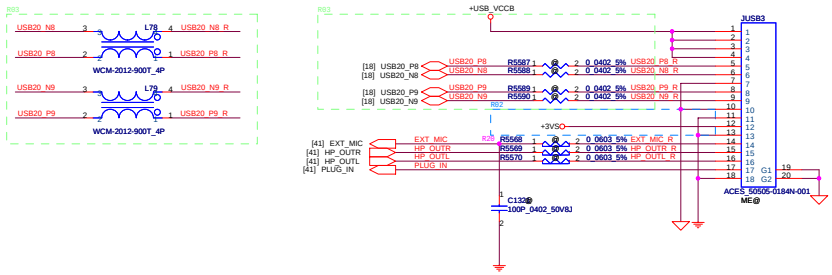
TP/B Connector



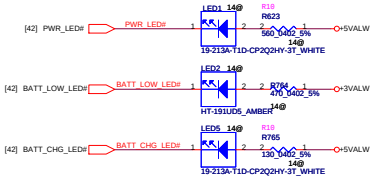
PWR/B Connector



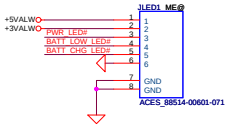
USB I/O Connector



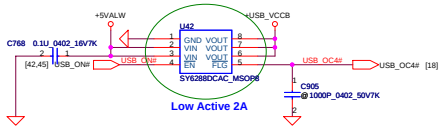
LED (For 14")



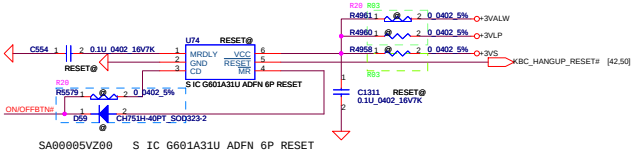
LED (For 15")



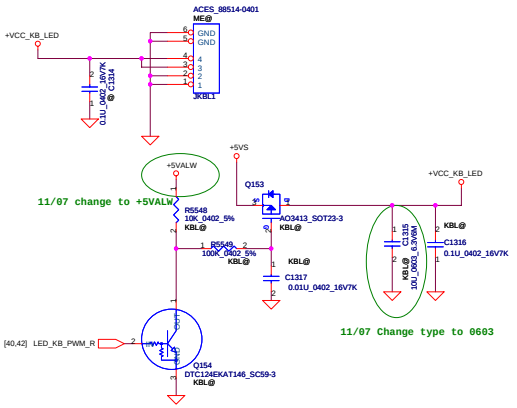
Right Side USB2.0 Port X 2 (USB/B)



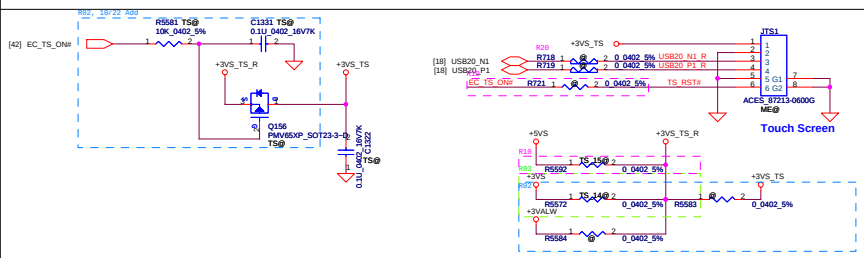
EC RESEST function



KB Lighting CONN.4pin



Touch Screen



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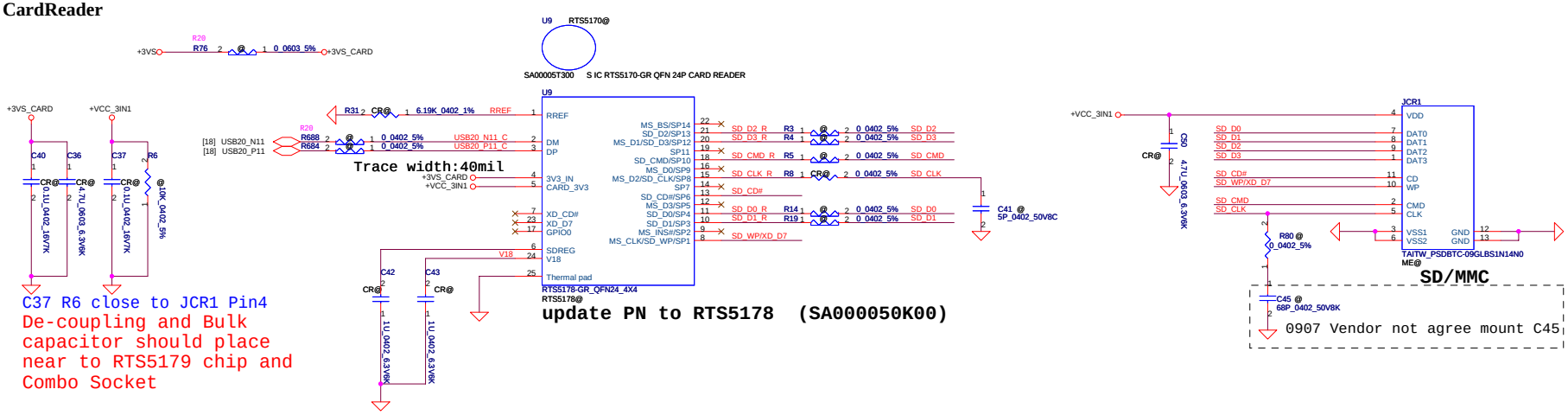
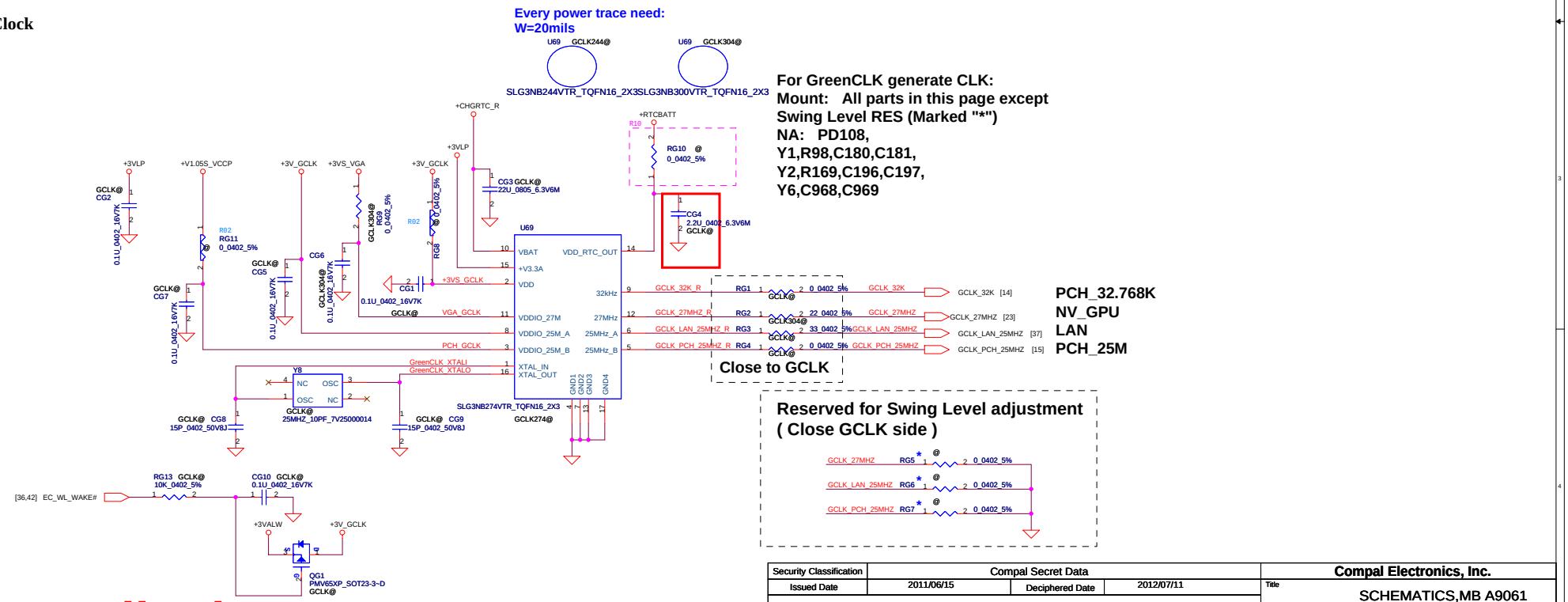
RTS5178 CardReader



Green Clock



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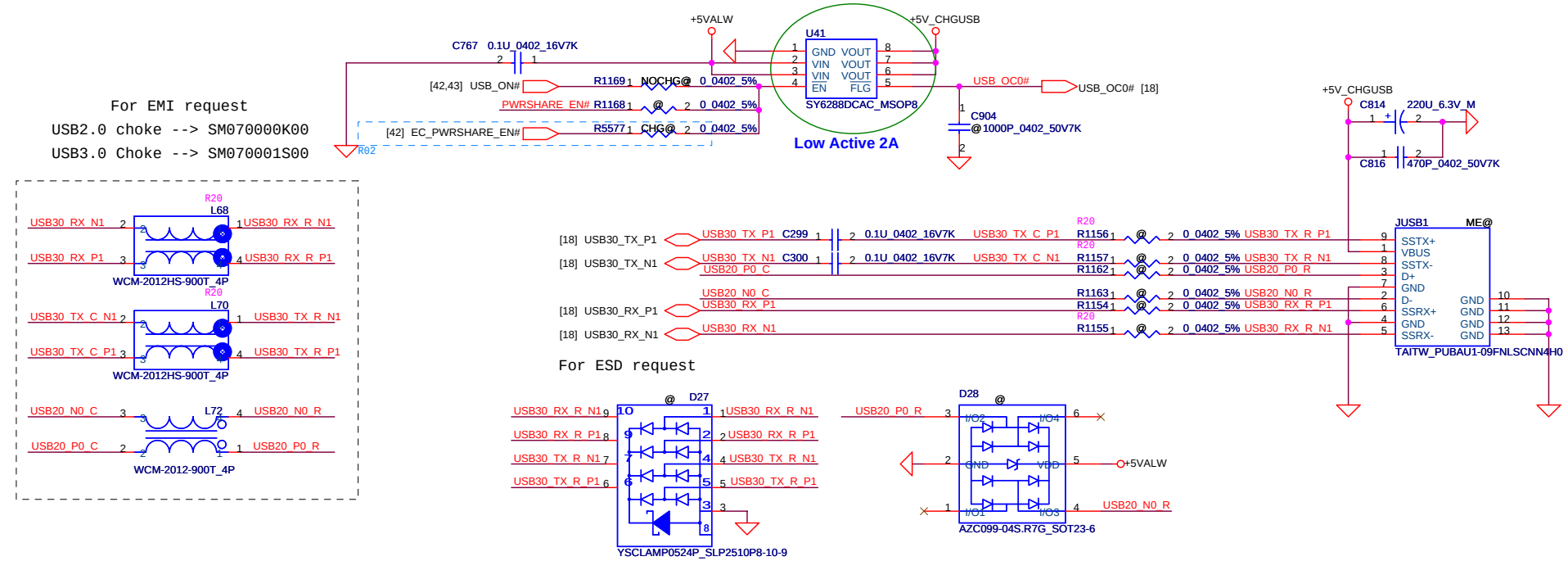
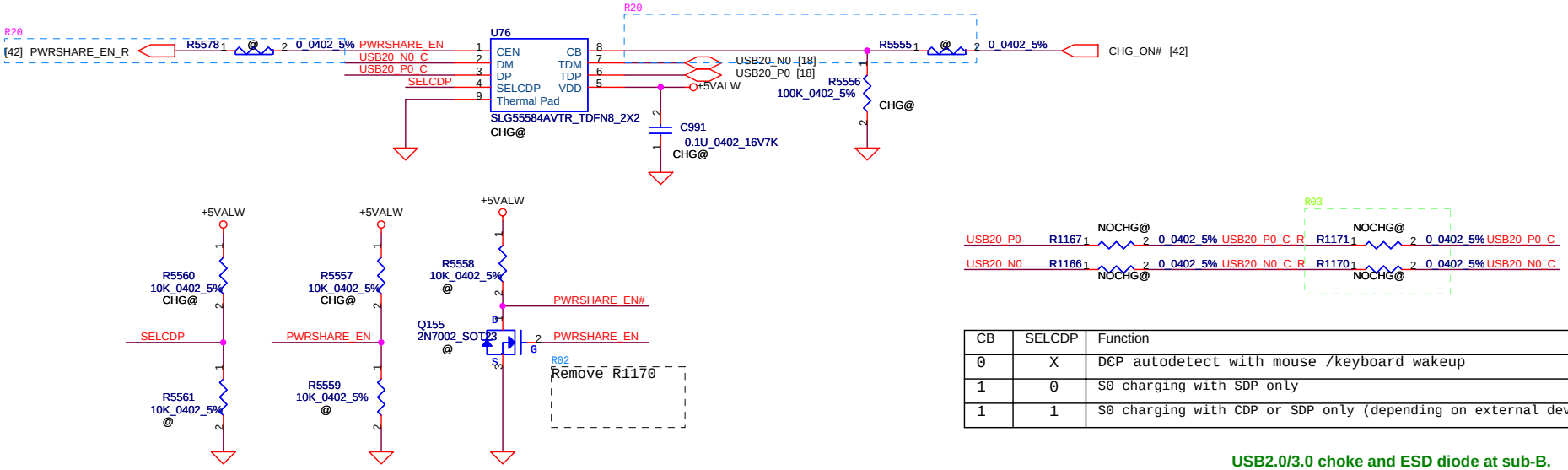
LEFT SIDE USB3.0 PORT X1



Left Side Charger USB3.0 Port



CB	SELCDP	Function
0	X	DCP autodetect with mouse /keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

USB2.0/3.0 choke and ESD diode at sub-B.

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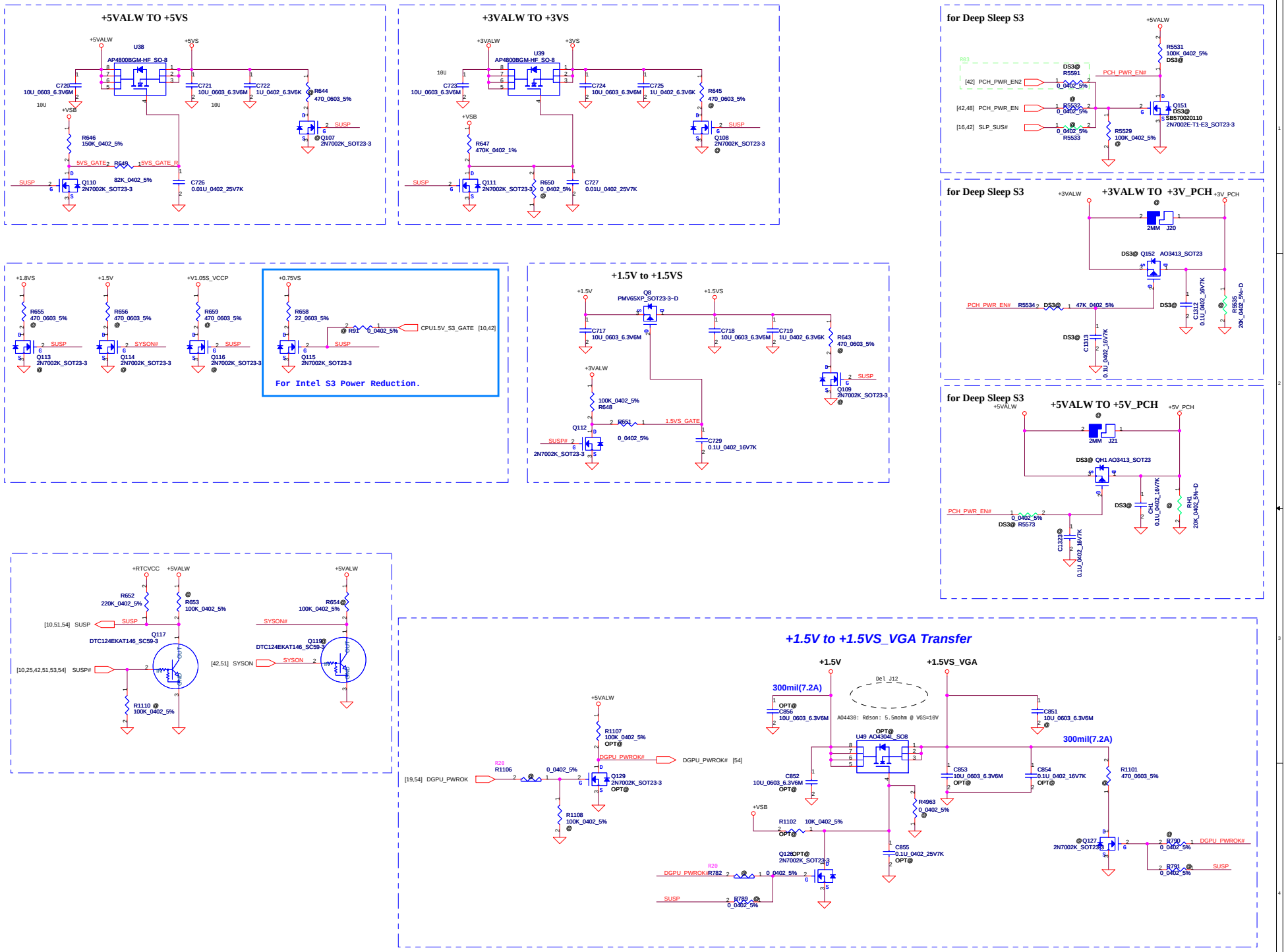

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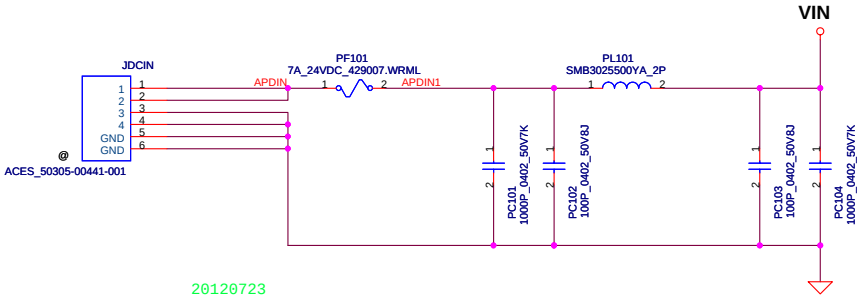
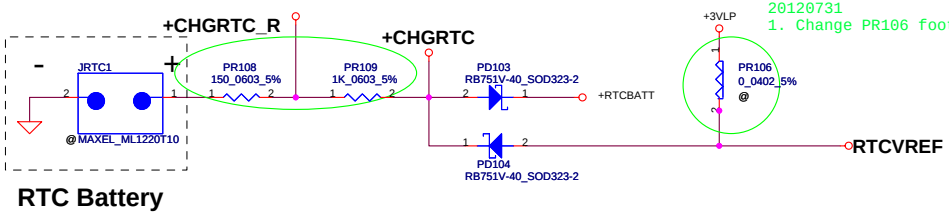


20120723
For all sku
1. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080
   Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080

20120731
1. Change PR106 footprint to R0402_0ohm-NEW



20120731
1. Add PR110 SD013000080 0_0603_5%
  Add PR111 SD013150080 150_0603_5%

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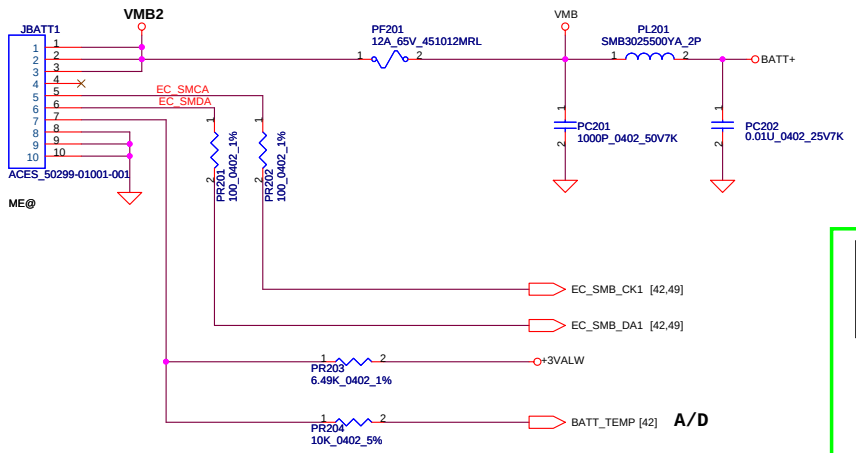
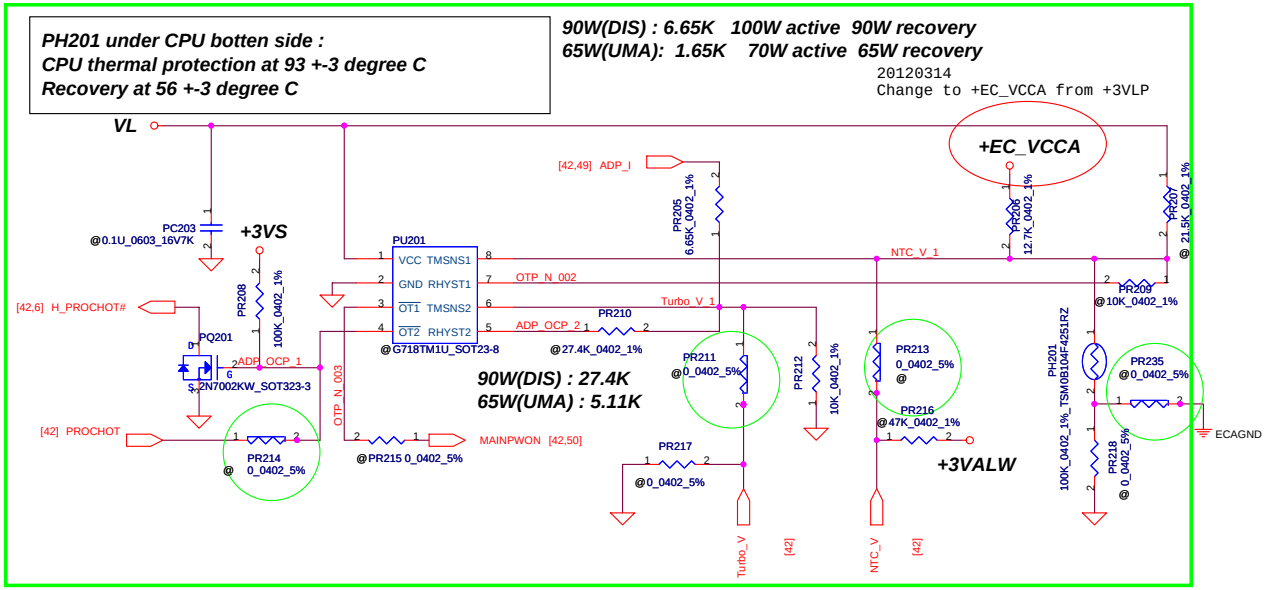
				Date: Monday, December 17, 2012 / Sheet 47 of 63

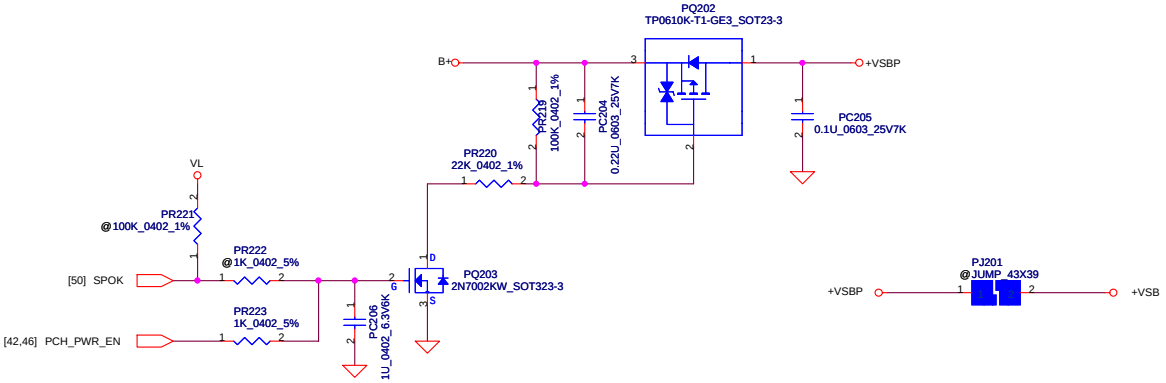


ADP_I need to write Charge Options Register (0x12H)=> bit6=1

0: IOUT is the 20x current amplifier output <default @ POR>
1: IOUT is the 40x current amplifier output



20120731
1. Change PR214,PR211,PR213 and PR235 footprint to R0402_0ohm-NEW



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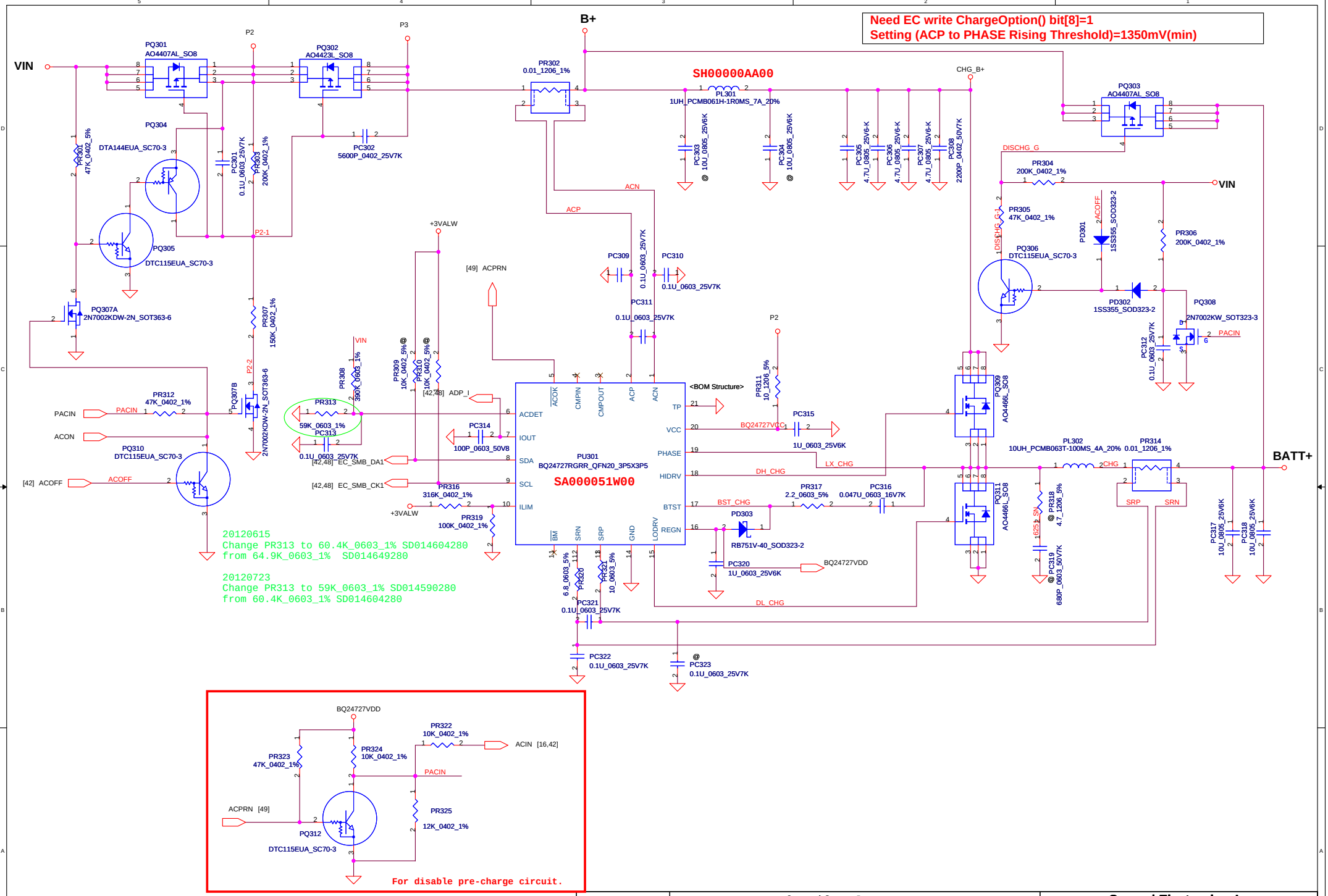

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Compal Electronics, Inc.

Title: **CHARGER**

Size: | Document Number: **Zx90** | Rev: **C**

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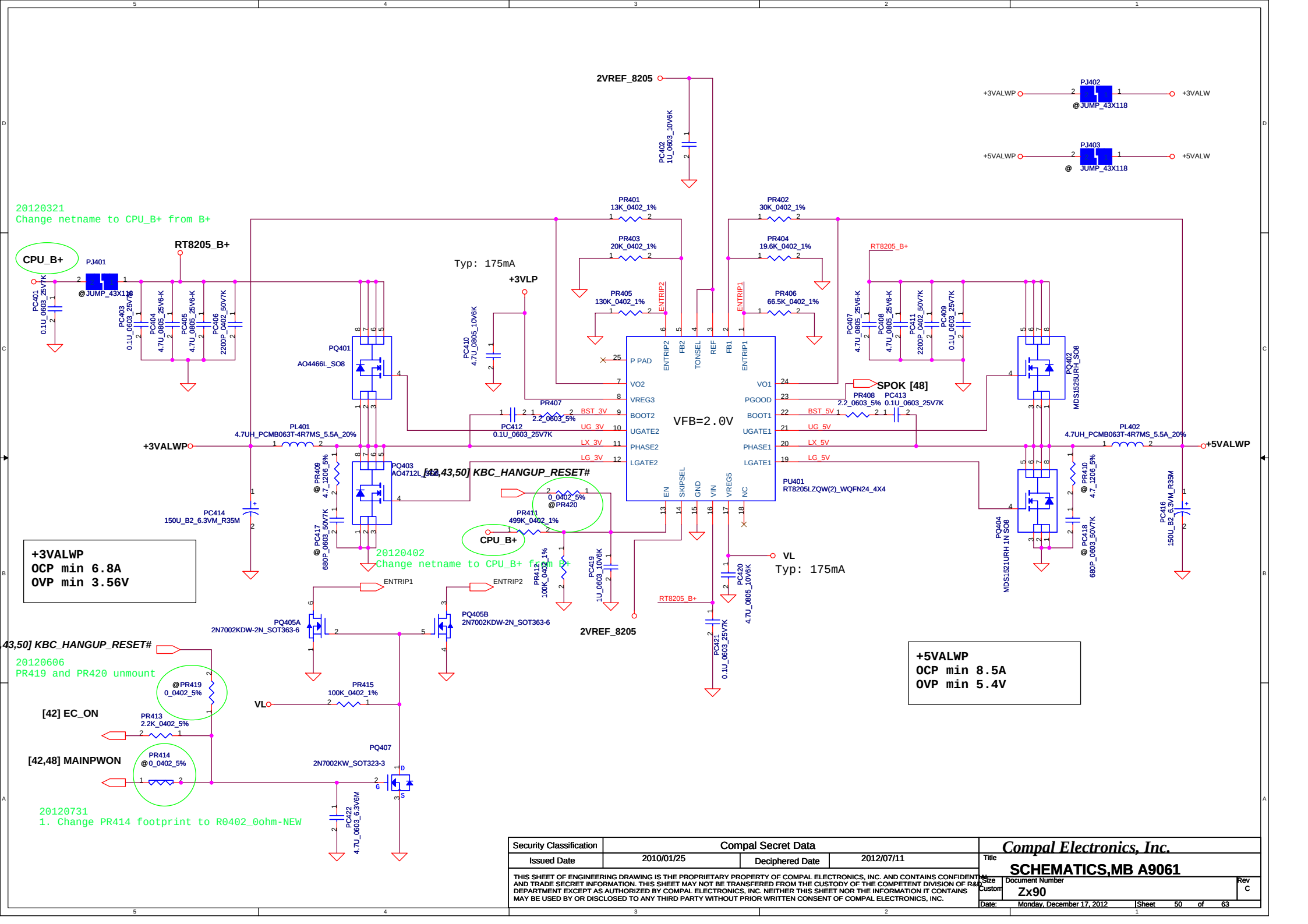

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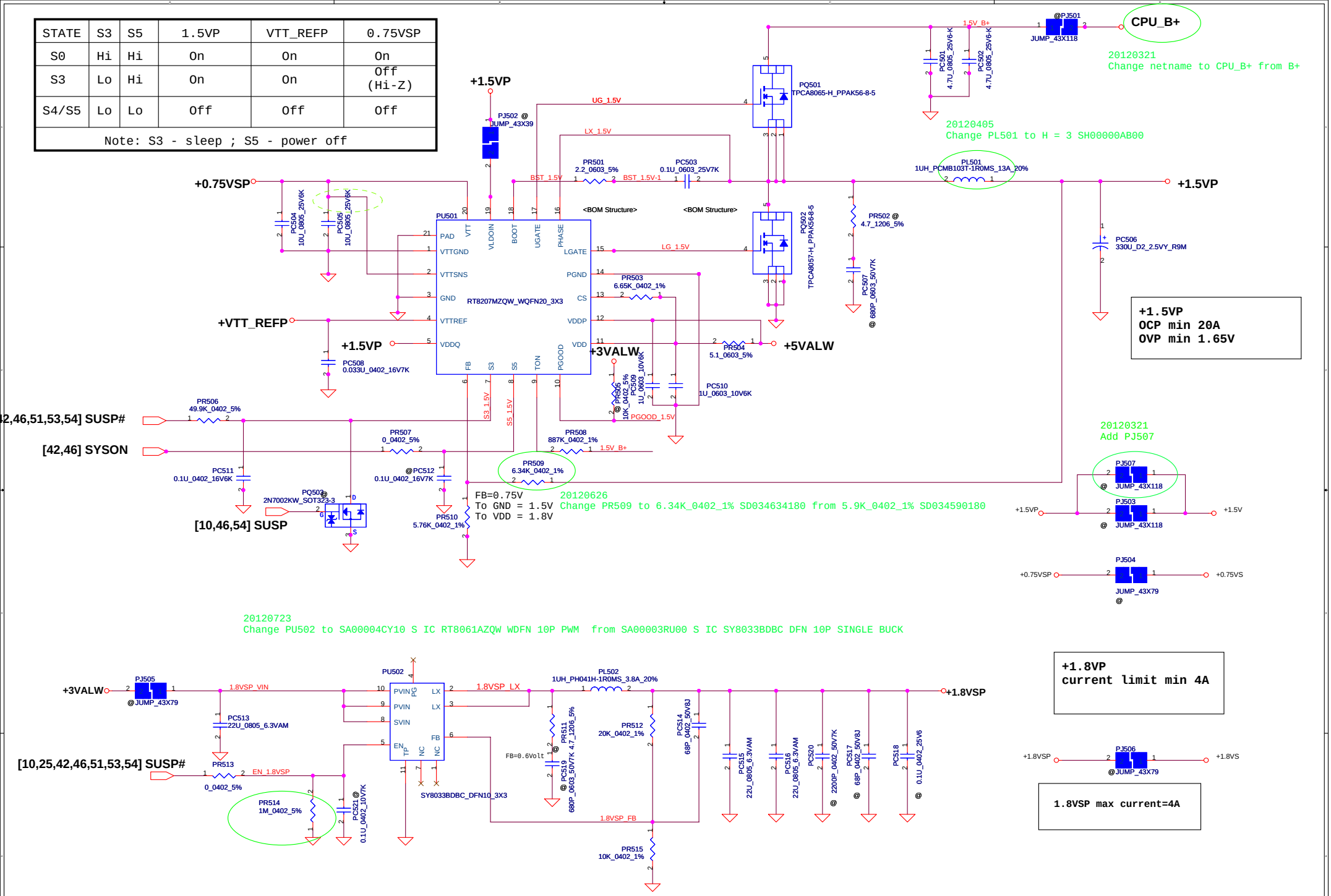
STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off
Note: S3 - sleep ; S5 - power off					



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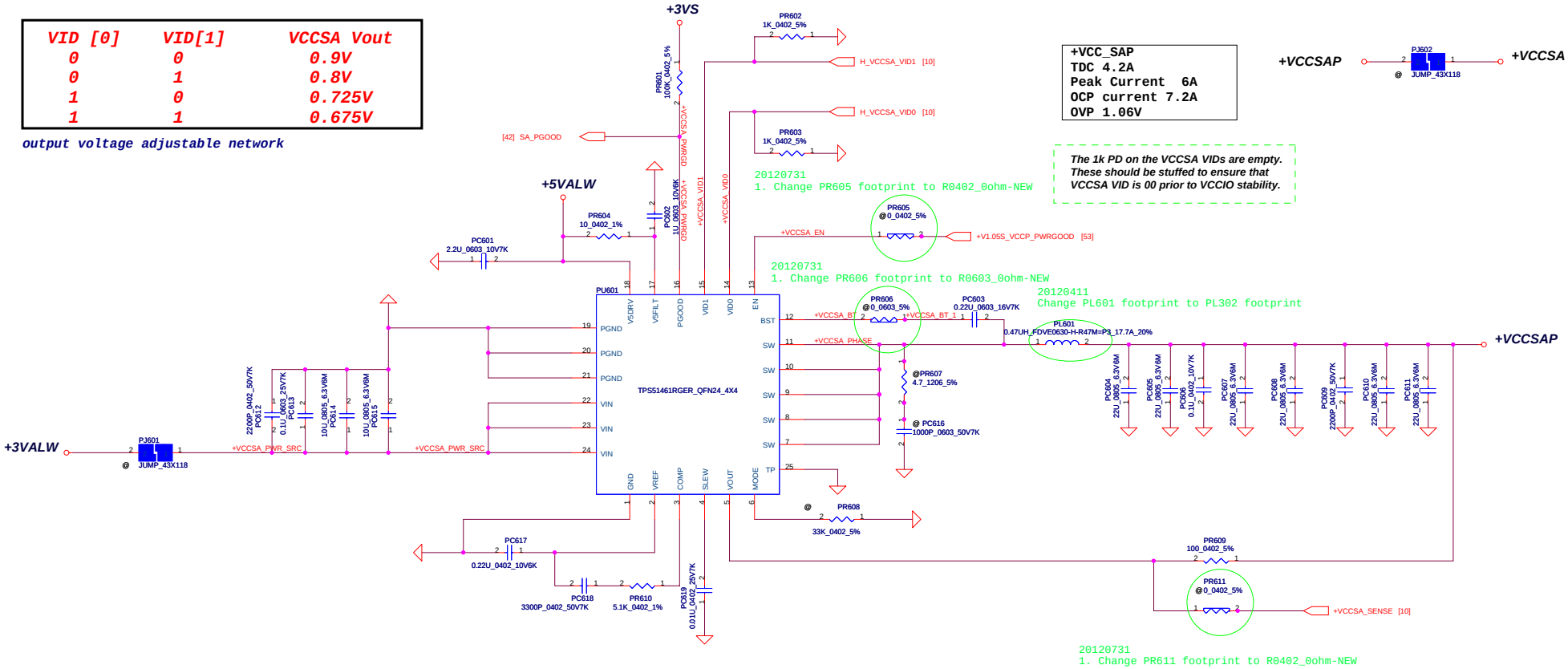
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A
OVP 1.06V

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



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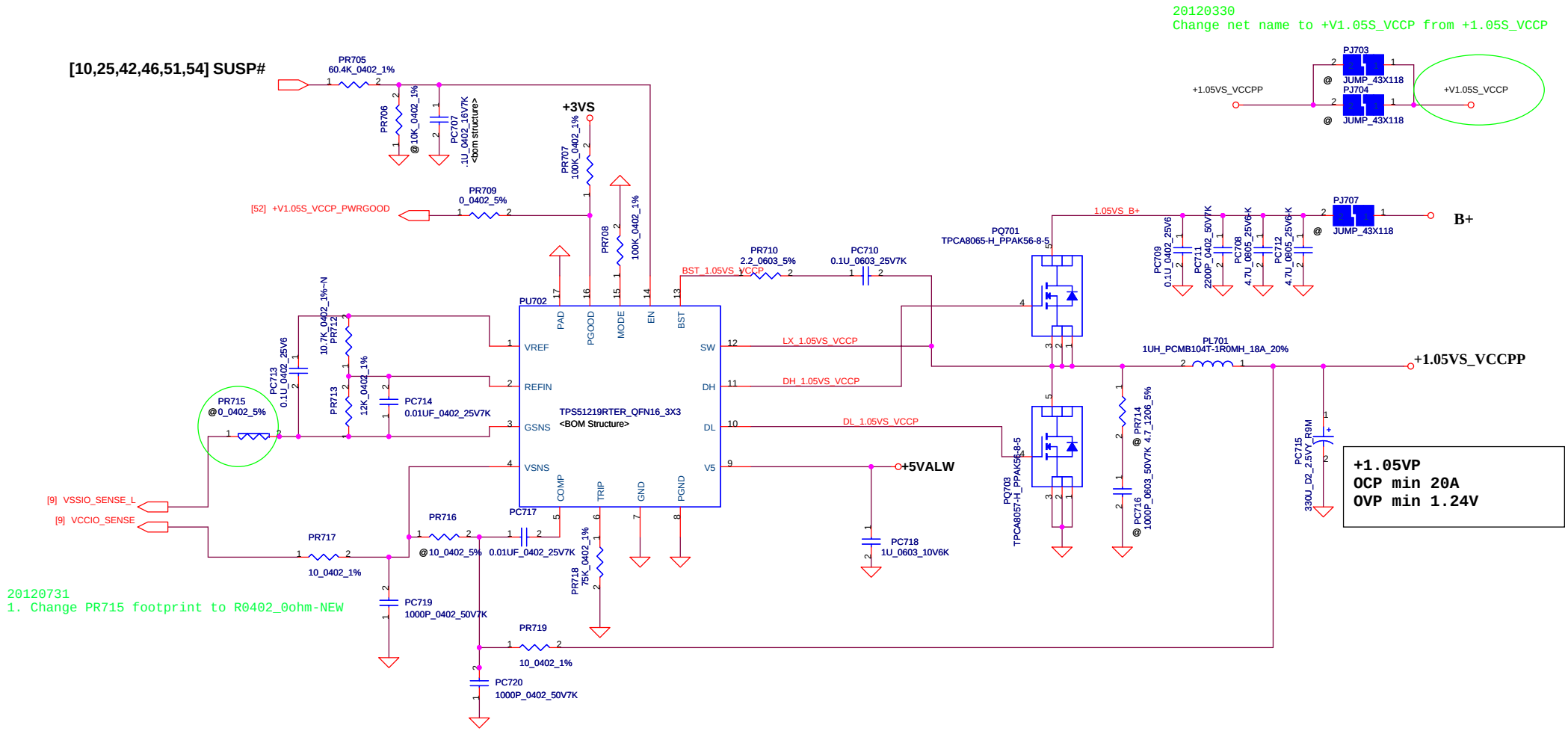

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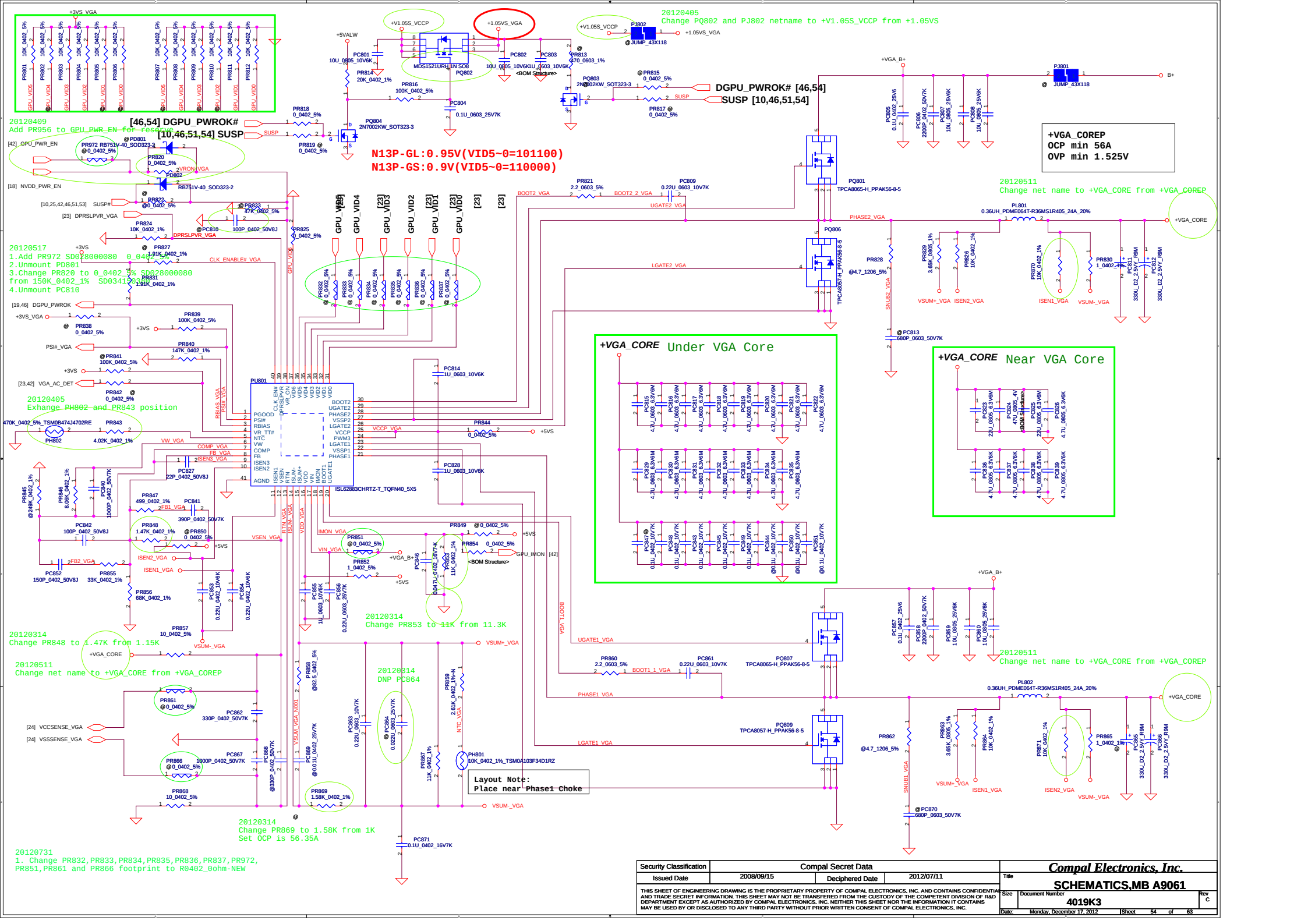

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Title: **SCHEMATICS,MB A9061**

Size: | Document Number: **4019K3** | Rev: C

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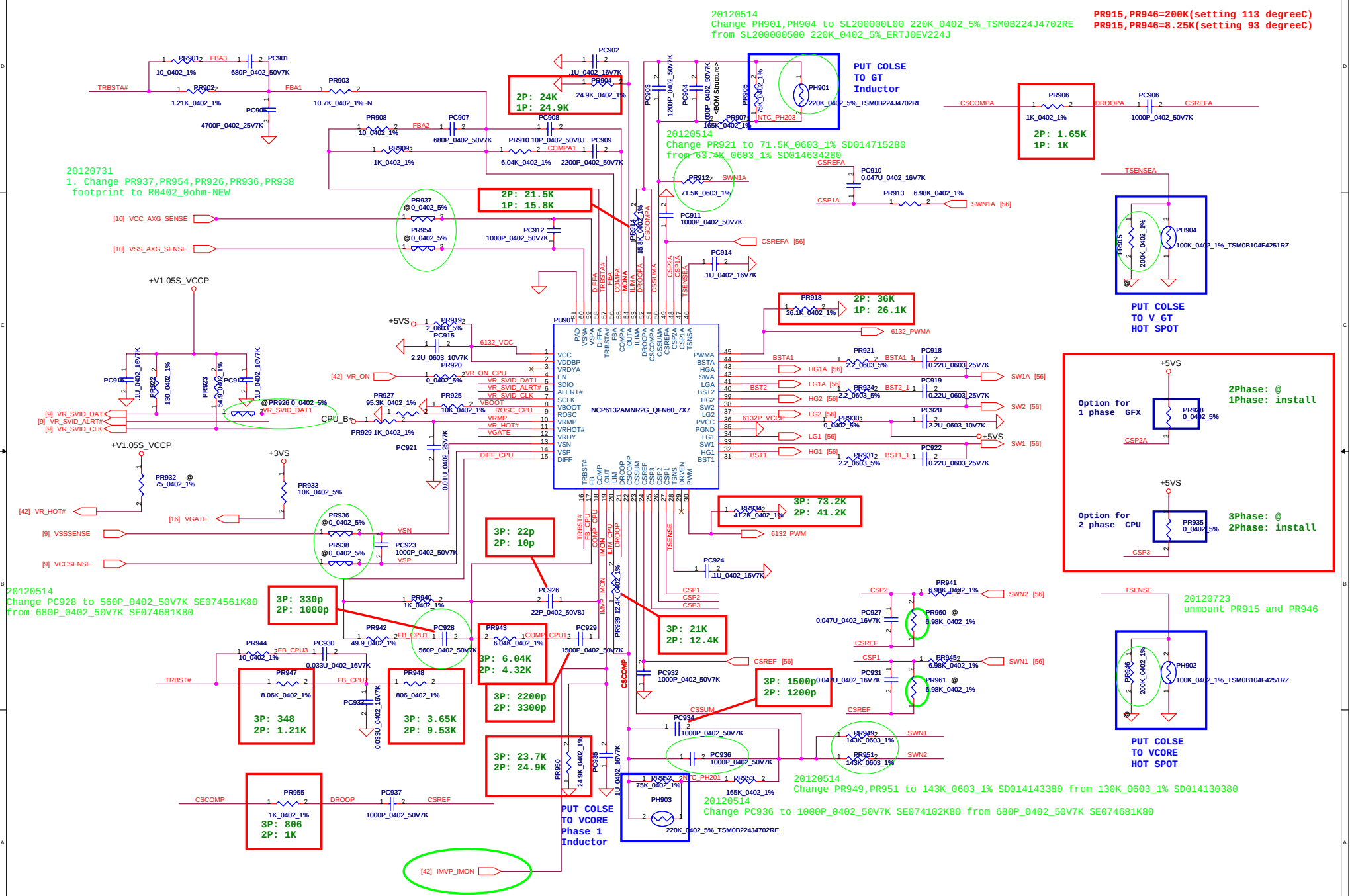

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Title: **SCHEMATICS,MB A9061**

Size: Custom | Document Number: C38-G series Chief River Schematic | Rev: C

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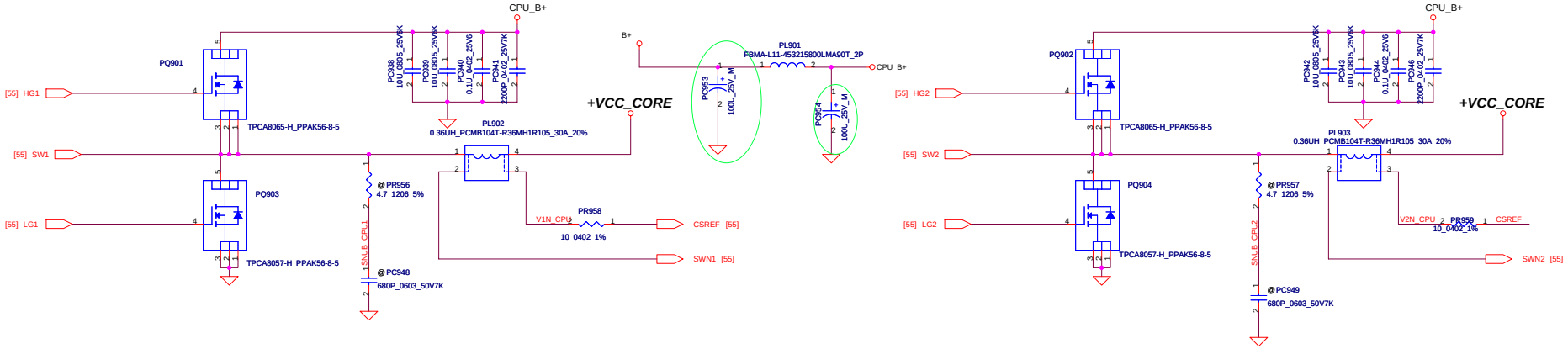
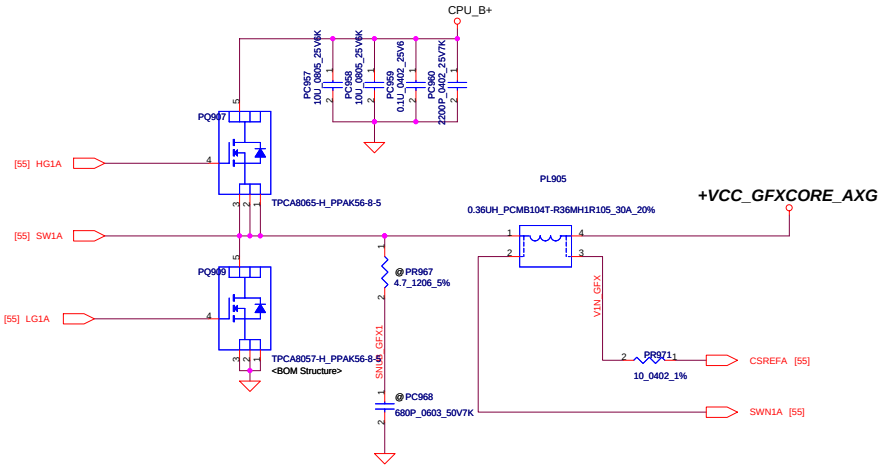


DC 35W CPU
VID1=1.05V
IccMax=53A
Icc_Dyn=43A
Icc_TDC=36A
R_LL=1.9m ohm
OCP~65A



DC 35W GT2
VID1=1.23V
IccMax=33A
Icc_Dyn=20.2A
Icc_TDC=21.5A
R_LL=3.9m ohm
OCP~40A

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Title: SCHEMATICS,MB A9061

Size: C | Document Number: C38-G series Chief River Schematic | Rev: C

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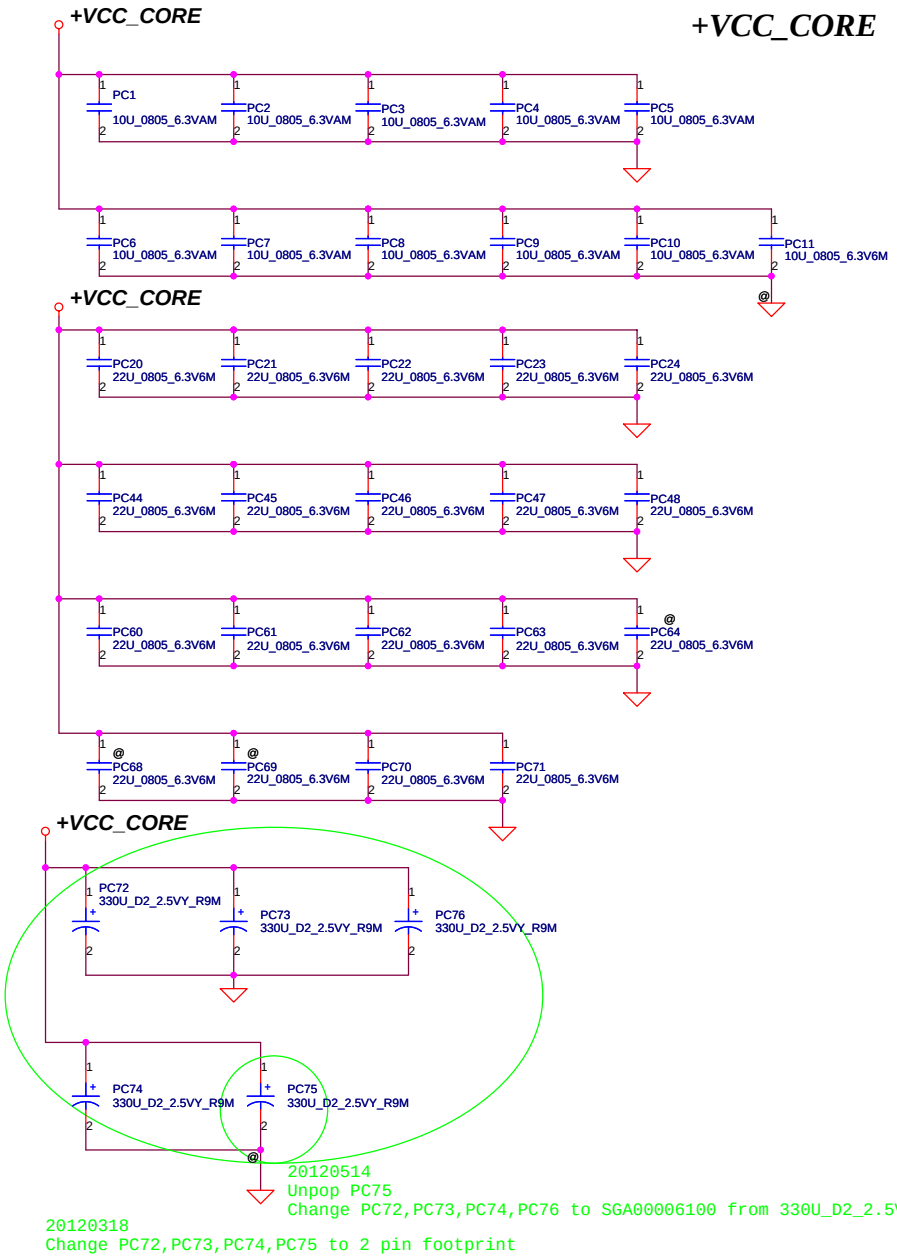
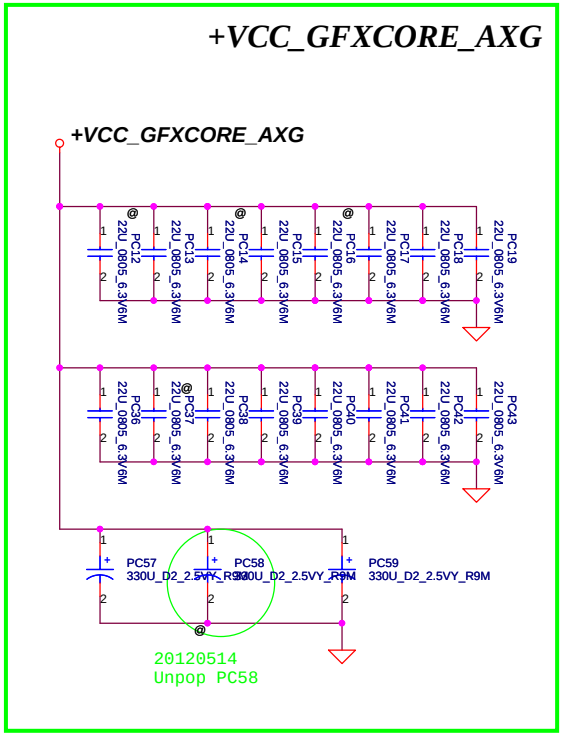


20120514
Unpop PC75
Change PC72,PC73,PC74,PC76 to SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680

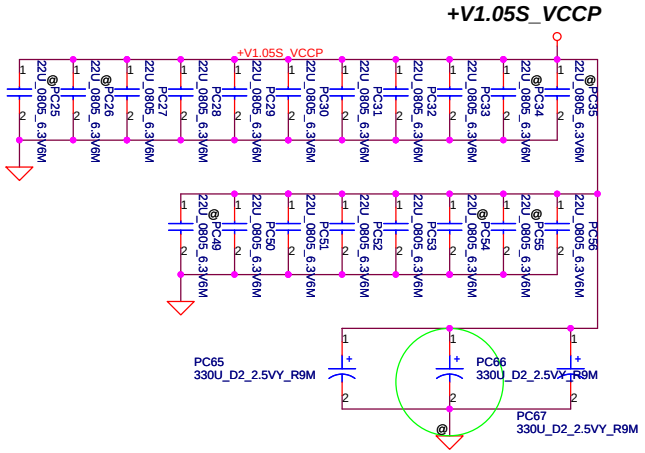
20120318
Change PC72,PC73,PC74,PC75 to 2 pin footprint



20120514
Unpop PC58

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites



20120514
Unpop PC66

Security Classification	Compal Secret Data		
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Title: **SCHEMATICS,MB A9061**

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For EC net name	P48	PR206 change pull high voltage to +EC_VCCA from +3VLP	20120316	EVT
2	Intersil advise	P54	1.Change PR848 to 1.47K SD000009480 from 1.15K 2.Unmount PC864	20120316	EVT
3	VGA IMON setting	P54	Change PR853 to 11K SD034110280 from 11.3K	20120316	EVT
4	set OCP is 56A	P54	Change PR869 to 1.58K (SD00000SJ80) from 1K	20120316	EVT
5	For 1.5V current	P51	Add PJ507 for 1.5V	20120321	EVT
6	For B+ layout	P55 P50 P51 P50	1.Change PC954 pull high to CPU_B+ from B+ 2.Change 3/5VALWP B+ input netname to CPU_B+ 3.Change 1.5VALWP B+ input netname to CPU_B+ 4.Change PR411 netname to CPU_B+ from B+	20120321	EVT
7	For HW net name	P53 P54	1.Change +1.05S_VCCP netname to +V1.05S_VCCP 2.Change PQ802.5 netname to +V1.05S_VCCP from +1.05VS	20120330	EVT
8	For HW power sequence	P54	1.Add control PU801 pin GPU_PWR_EN and reserve PR956 0_0402_5% 2.Change PR820 to SD034150380 150K_0402_1% from 100K 3.Change PC810 to SE071101J80 100P_0402_50V8J from 0.1u	20120330	EVT
9	For Intersil advise	P54	Change PR853 pull down netname to gnd	20120409	EVT
10	For IMON design	P55	Change PU901 to NCP6132A from ISL95836	20120412	EVT
11	For layout design	P54	1.Del PJ803 PJ804 2.Change net name to VGACORE from VGACOREP	20120511	DVT
12	For 1.05V, GFX_CORE,CPU_CORE design fine tune	P57	Unpop PC58, PC66,PC75 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
13	For CPU_CORE design fine tune and ON advise	P57	Change PC72,PC73,PC74,PC76 to S POLY C 330U 2V M D2 ESR9M SGA00006100 from 330U_D2_2.5VY_R9M SGA00002680	20120514	DVT
14	For CPU_CORE design fine tune and ON advise	P55	1.Change PC928 to 560P_0402_50V7K SE074561K80 from 680P_0402_50V7K SE074681K80 2.Change PR949,PR951 to 140K from 130K 3.Change PR912 to 71.5K_0603_1% SD014715280 from 63.4K_0603_1% SD014634280 4.Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
15	For material EOL	P55	Change PH901,PH904 to SL200000L00 220K_0402_5%_TSM0B224J4702RE from SL200000500 220K_0402_5%_ERTJ0EV224J	20120514	DVT
16	For HW VGA power sequence	P54	Add PR972 SD028000080 0_0402_5% Unmount PD801 Change PR820 to 0_0402_5% SD028000080 from 150K_0402_1% SD034150380 Unmount PC810	20120516	DVT

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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
17	For HW reset function	P50	1.Add PR420 SD028000080 0_0402_5% for reserve 2 reserve.PR419 and PR420	20120606	PVT
18	For ACDET function	P49	1.Change PR313 to 60.4K_0603_1% SD014604280 from 64.9K_0603_1% SD014649280	20120615	PVT
19	For HW Grenn clock UMA sku trial tun	P47	1. unmount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120625	PVT
20	For ACDET function	P49	1.Change PR313 to 59K_0603_1% SD014590280 from 60.4K_0603_1% SD014604280	20120705	PVT
21	For VR_HOT	P55	1.unmount PR915 and PR946	20120705	PVT
22	For HW Grenn clock	P47	1. mount PD103 2. Change PR108 to 150_0603_5% SD013150080 from 560_0603_5% SD013560080 Change PR109 to 1K_0603_5% SD013100180 from 560_0603_5% SD013560080	20120723	SVT
23	For material issue	P51	1.Change PU502 to SA00004CY10 S IC RT8061AZQW WDFN 10P PWM from SA00003RU00 S IC SY8033BDBC DFN 10P SINGLE BUCK	20120723	SVT

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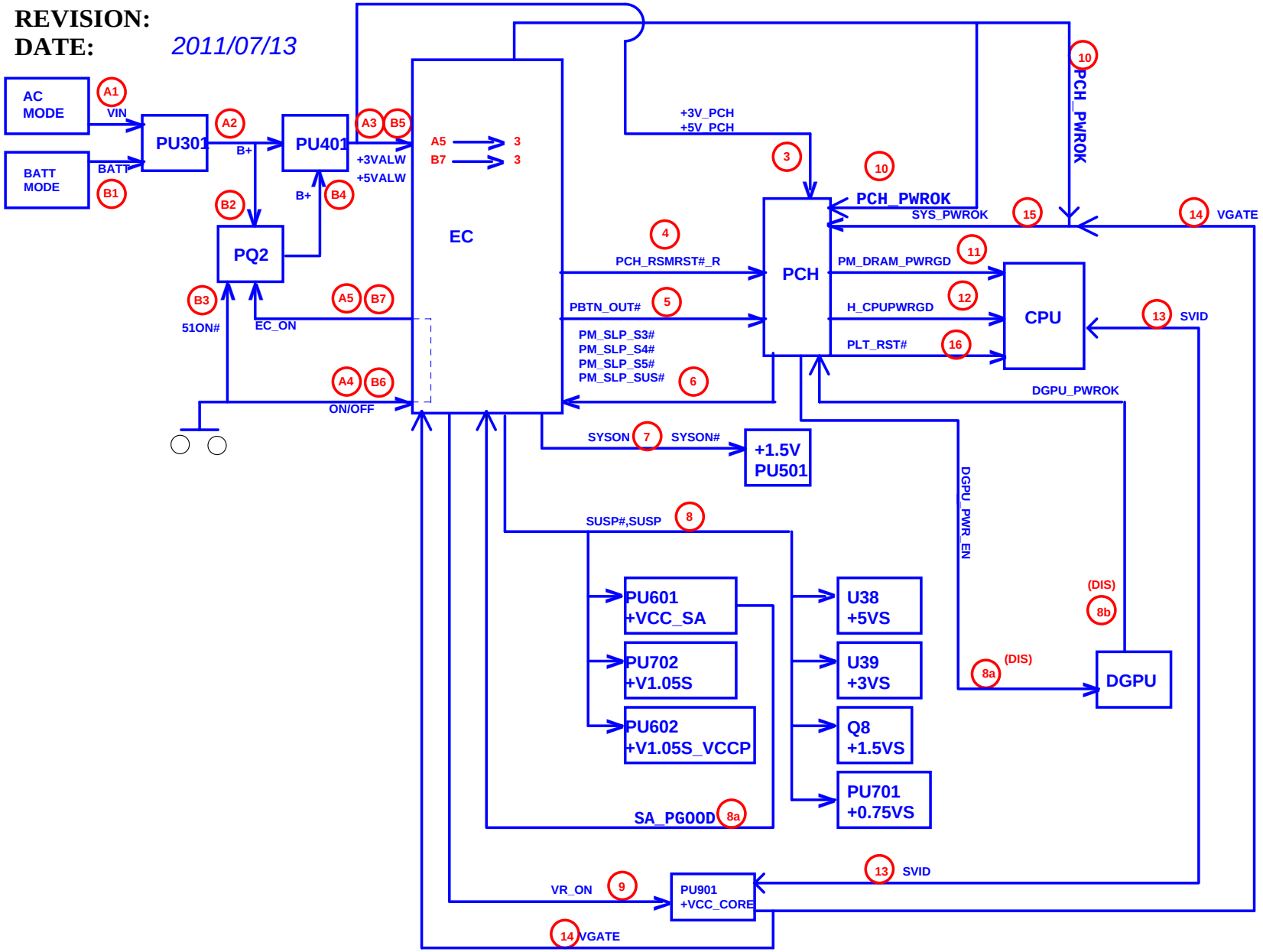
COMPAL CONFIDENTIAL

MODEL NAME: *Power Sequence Block Diagram*
PCB NAME: *LA-7981P*
REVISION:
DATE: *2011/07/13*



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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Initial			5/7	DVT
2	For Green CLK and Crystal co-lay better layout	P14 P15 P23	Delete R176,R1381 and RV232	5/7	DVT
3	For Change Audio Woofer MOSFET from Dual to single channel	P15	Changer Part from SB00000EO10 to SB00000EN00	5/7	DVT
4	For OVERT# Glitch issue at Power on status	P23	Add QV9	5/7	DVT
5	For BT&WLAN Combo Card	P36	to modify R897 value from 0 ohm to 1K ohm add BT_DISABLE_F_R on JWLN1.51 add R5580	5/8	DVT
6	For Factory request and cost down LVDS PIN Define	P33	To Modify LVDS PIN Define	5/8	DVT
7	For USB Charger mode control request	P45 P42	To Add PWRSHARE_EN_R on U31.38 To Add EC_PWRSHARE_EN# on U31.74 add R5577 and R5578, delete CHG_ON#	5/8	DVT
8	To change Reset IC G601	P42	to change R4959 value from 200K ohm to 0 ohm add R5579 0 ohm	5/8	DVT
9	Reserved Touch Screen Power Control	P42 P43	add R5581,C1331,R5572,R5583,R5584 and Q156 add EC_TS_ON on U31.66 add +3VS_TS,+3VS_TS_R	5/8	DVT
10	To change Speaker PIN define for ME routing request	P41	SPK_L2+ R1556 net in JSPK1.1 SPK_L1- R1554 net in JSPK1.2 SPK_R1- R1555 net in JSPK1.3 SPK_R2+ R1553 net in JSPK1.4	5/8	DVT
11	for Realtek Vendor recommand	P41	R1123,C1134 close to U50.47 R5582,R1559 and C1135 Close to U73.1 EXT_MIC_R	5/8	DVT
12	for ME request	P39	To Modify H21,H7,H18 PCB Footprint as below H21 from H_3P3 to H_4P6 H7 from H_2P8 to H_3P0 H18 from H_3P3 to H_3P9N	5/8	DVT
13	for LAN Clock be better	P37	change C990 value from 5PF to 0 ohm.	5/9	DVT
14	for Audio Vendor recommand	P43	change JUSB3.11 from GND to +3VS change JUSB3.12 from +3VS to AGND	5/10	DVT
15	for Crystal finetune Capacitor	P43	C180,C181 from 18PF to 12PF	5/16	DVT
16	for DVT Board ID request	P42	R695 from 33K to 18K	5/17	DVT
17	for PVT request	P37	Change Reference from C990 to R5585	5/23	PVT
18	for Surge request	P38	C1325,C1326,C1327 change package from 0402 to 0603	5/23	PVT
19	for Reset IC function	P42, P50,P43	add R612,PR420,R4960,R4961 Delete R4959	5/24	PVT

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Item	Reason for change	PG#	Modify List	Date	Phase
20	for USB2.0 Port 0 TLC fine tune	P45	add R1170,R1171	5/29	PVT
21	for INTEL Combo card BT off	P36 P19	add R893,R894 1Kohm ,change R897 to 0 ohm change net name from PCH_GPIO36 to INTEL_BT_OFF# add INTEL_BT_OFF#_R JWLN1.51 chnage NET from BT_DISABLE_F_R to INTEL_BT_OFF#_R	6/5	PVT
22	for LVDS prevent short EC DISPOFF#	P33	R447 change value from no stuff to stuff 0ohm	6/12	PVT
23	for VSB and PCH Power rail control issue	P42 P46	add R5586 and R5591	6/21	PVT
24	add common choke for USB port 8, port 9	P43	add L78,L79,R5587,R5588,R5589,R5590	6/21	PVT
25	no need reserved C1330	P38	remove C1330	6/21	PVT
26	for PVT Board ID request	P42	R695 from 18K to 8.2K	6/21	PVT
27	for Surge modify	P38	DL6 change Part from SCV00001C00 to SCV00001D00	6/21	PVT
28	for Crystal finetune Capacitor	P14 P37	C180,C181 change value from 12P to 18P C1204,C1205 change value from 27P to 12P	6/25	PVT
29	for SMT Request	P23	LV7 change value from KC_FBMA-10-100505-300T_2P to 0ohm_0402	07/11	SVT
30	for Vendor recommand	P23	add RG10 0ohm	07/19	SVT
31	for Touch Screen request	P43	add R5592,R721 0 ohm,	07/25	SVT
32	for Green CLK request	P44	add QG1,RG13,CG10	8/1	SVT
33	for LED Brightness	P44	modify R623,R765 value from 300 ohm to 560 ohm	8/1	SVT
34	for reduce component count	P10 P	Modify footprint to jumper R69 to J14 R277 to J16	8/1	SVT
35	for SVT Board ID request	P42	R695 from 8.2K to 0 ohm	8/1	SVT

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Item	Reason for change	PG#	Modify List	Date	Phase
36	for EMI Request	P45	not stuff R1154,R1155,R1156,R1157 Stuff L68,L70	8/1	SVT
37	for Remove ODD Zero Power Function	P40	Q99,Q100 R552,R675,C607 not stuff on MB		

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